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Memory Products	

82LS16

256-bit TTL bipolar RAM

DESCRIPTION

The 82LS16 is a Read/Write memory array which features 3-State outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82LS16 has fast Read access and Write cycle times, as well as low power requirements and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Ordering codes are listed in the Ordering Information Table

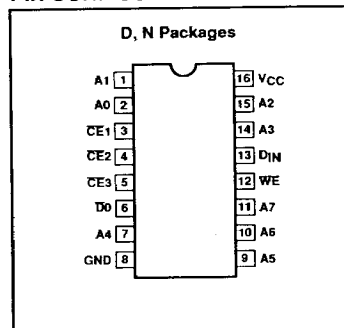
APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

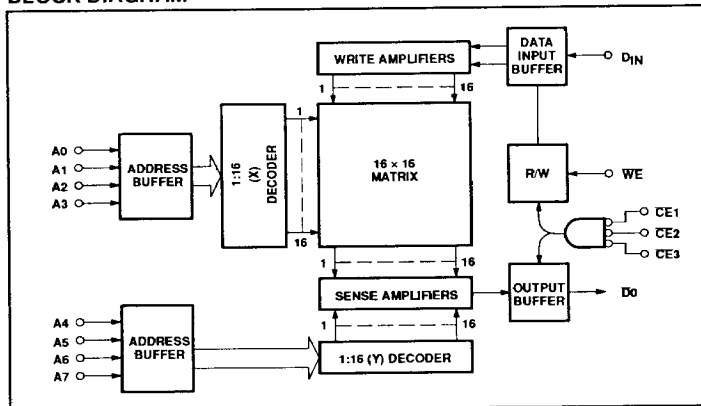
FEATURES

- Address access time: 40ns max
- Write cycle time: 45ns max
- Power dissipation: 0.98mW/bit typ
- Input loading: -100µA max
- Output follows complement of data input during Write
- On-chip address decoding
- Three Chip Enable inputs
- Output: 3-State
- Schottky clamped
- TTL compatible

PIN CONFIGURATION



BLOCK DIAGRAM



256-bit TTL bipolar RAM (256 × 1)**82LS16****ORDERING INFORMATION**

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N82LS16 N
16-Pin Plastic Small Outline 300mil-wide	N82LS16 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open-collector)	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_{amb} \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS ⁵	LIMITS			UNIT
			MIN	TYP ¹	MAX	
Input voltage²						
V_{IH}	High	$V_{CC} = 5.25\text{V}$	2.0			V
V_{IL}	Low	$V_{CC} = 4.75\text{V}$			0.8	V
V_{IC}	Clamp ³	$V_{CC} = 4.75\text{V}$, $I_{IN} = -12\text{mA}$		-1.0	-1.5	V
Output voltage²						
V_{OH}	High	$V_{CC} = 4.75\text{V}$ $I_{OH} = -3.2\text{mA}$	2.6			V
V_{OL}	Low ⁴	$I_{OL} = 16\text{mA}$		0.35	0.45	V
Input current³						
I_{IH}	High	$V_{CC} = 5.25\text{V}$ $V_{IN} = 5.5\text{V}$		1	25	μA
I_{IL}	Low	$V_{IN} = 0.45\text{V}$		-10	-100	μA
Output current						
I_{OZ}	Hi-Z state ⁵	$V_{OUT} = 5.5\text{V}$ $V_{OUT} = 0.45\text{V}$		1	40	μA
I_{OS}	Short circuit ⁶	$V_{CC} = 5.25\text{V}$, $V_O = 0\text{V}$	-15	-1	-40	μA
Supply current⁷						
I_{CC}		$V_{CC} = 5.25\text{V}$		50	70	mA
Capacitance						
C_{IN}	Input	$V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0\text{V}$		8		pF

NOTES:

- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = +25^{\circ}\text{C}$.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time
- Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
- Duration of the short-circuit should not exceed 1 second.
- I_{CC} is measured with the Write Enable and Memory Enable inputs grounded, all other inputs at 0.45V, and the output open.

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TRUTH TABLE

MODE	CE*	WE	D _{IN}	D _{OUT}
Read	0	1	X	Stored Data
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disable	1	X	X	Hi-Z

* "0" = All CE inputs Low; "1" = One or more CE inputs High. X = Don't care

AC ELECTRICAL CHARACTERISTICS

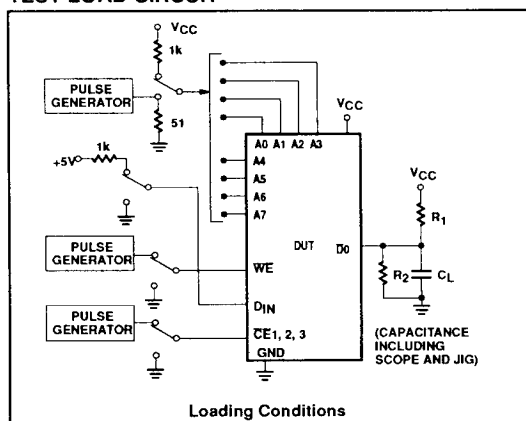
R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF, 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				MIN	TYP ¹	MAX	
Access time							
t _{AA}	Address	Output	Address		30	40	ns
t _{CE}	Chip Enable	Output	Chip Enable		15	25	ns
Disable time²							
t _{CD}		Output	Chip Enable		15	25	ns
t _{WD}	Valid time	Output	Write Enable		30	40	ns
Setup and hold time							
t _{WSA} ³	Setup time	Write Enable	Address	0	-5		ns
t _{WHA}	Hold time	Write Enable	Address	0	-5		ns
t _{WSD}	Setup time	Write Enable	Data in	25	15		ns
t _{WHD}	Hold time	Write Enable	Data in	0	-5		ns
t _{WSC}	Setup time	Write Enable	CE	0	-5		ns
t _{WHC}	Hold time	Write Enable	CE	0	-5		ns
Pulse width⁴							
t _{WP} ⁵	Write Enable			25	15		ns

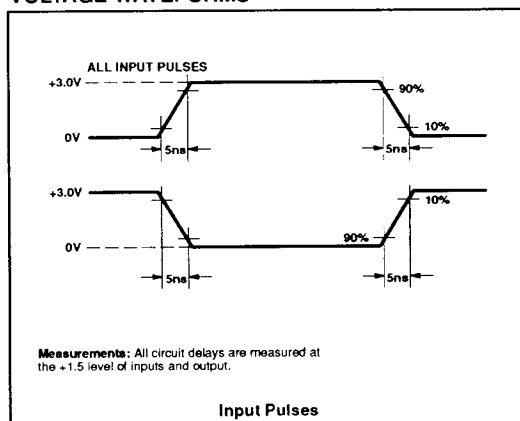
NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. Measured at a delta of 0.5V from the logic level with R₁ = 750Ω, R₂ = 750Ω and C_L = 5pF.
3. Measured with minimum t_{WP}.
4. Minimum required to gurarantee a Write into the slowest bit.
5. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



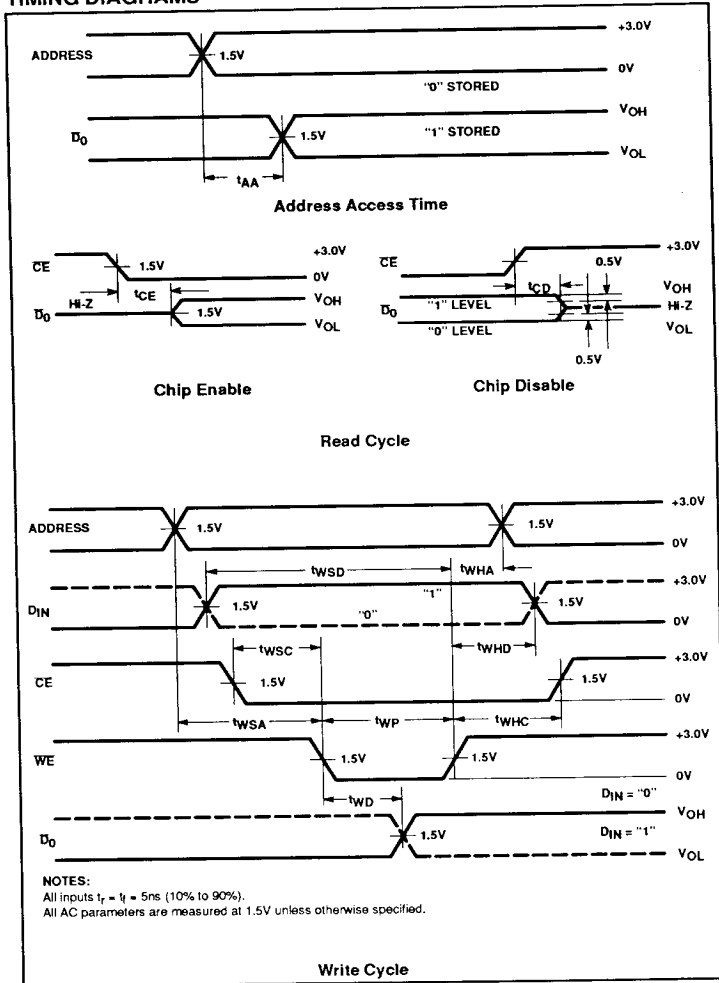
VOLTAGE WAVEFORMS



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TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in Off-State.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WHP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WDC}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.