

DESCRIPTION

The 82LS180 and 82LS181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82LS180 and 82LS181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or 3-state outputs for optimization of word expansion in bused organizations.

The 82LS180 and 82LS181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82LS180/181, F or N, and for the military temperature range (-55°C to +125°C) specify S82LS180/181, F.

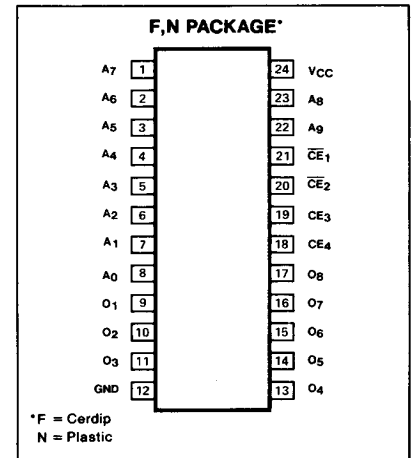
FEATURES

- Address access time:
N82LS180/181: 175ns max
S82LS180/181: 225ns max
- Power dissipation: 37µW/bit typ
- Input loading:
N82LS180/181: -100µA max
S82LS180/181: -150µA max
- On-chip address decoding
- Output options:
82LS180: Open collector
82LS181: 3-state
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

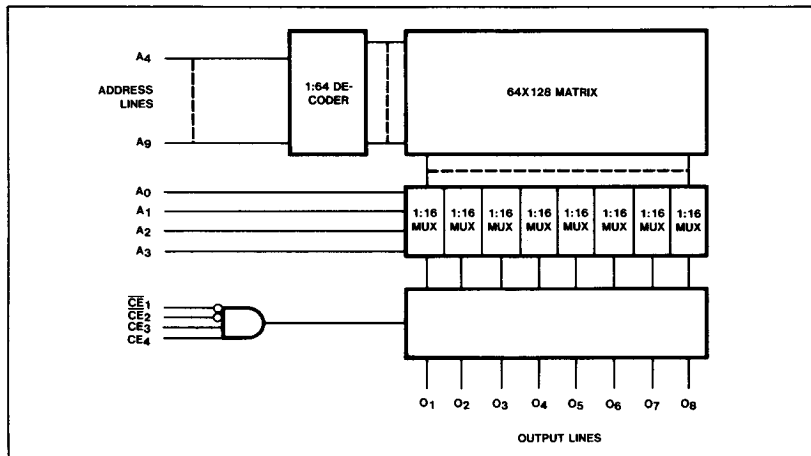
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _{OH} Output voltage		Vdc
High (82LS180)	+5.5	
Off-state (82LS181)	+5.5	
T _A Temperature range		°C
Operating		
N82LS180/181	0 to +75	
S82LS180/181	-55 to +125	
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82LS180/181: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82LS180/181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ¹	N82LS180/181			S82LS180/181			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0	-0.8	.85 -1.2	2.0	-0.8	.80 -1.2	V
V _{OL} V _{OH}	Output voltage Low High (82LS181) I _{OUT} = 4.8mA CE ₁ = low, I _{OUT} = -1mA, CE ₂ = low, CE ₂ = high, CE ₄ = high, high stored	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{OLK} I _{O(OFF)}	Output current Leakage (82LS180) Hi-Z state (82LS181) CE ₁ = CE ₂ = HIGH CE ₃ = CE ₄ = LOW			V _{OUT} = 5.5V 40			60	μA
				V _{OUT} = 0.5V -40			-60	μA
				V _{OUT} = 5.5V 40			60	μA
I _{OS}	Short circuit (82LS181) CE ₁ = CE ₂ = LOW, CE ₂ = CE ₃ = HIGH	-10		-70	-10		-85	mA
I _{CC}	V _{CC} supply current		60	80	60		85	mA
C _{IN} C _{OUT}	Capacitance Input Output V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		5 8			pF

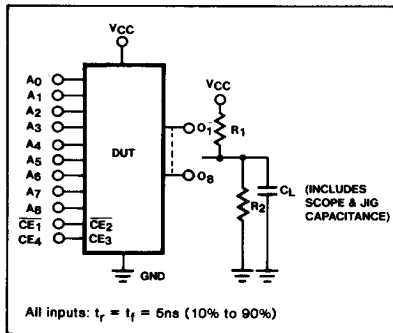
AC ELECTRICAL CHARACTERISTICS R₁ = 1kΩ, R₂ = 2kΩ, C_L = 30pF
 N82LS180/181: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82LS180/181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82LS180/181			S82LS180/181			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T _{AA} T _{CE}	Access time Output Output	Address Chip enable		100 35	175 60		100 35	225 80	ns
T _{CD}	Disable time Output	Chip disable		35	50		35	70	ns

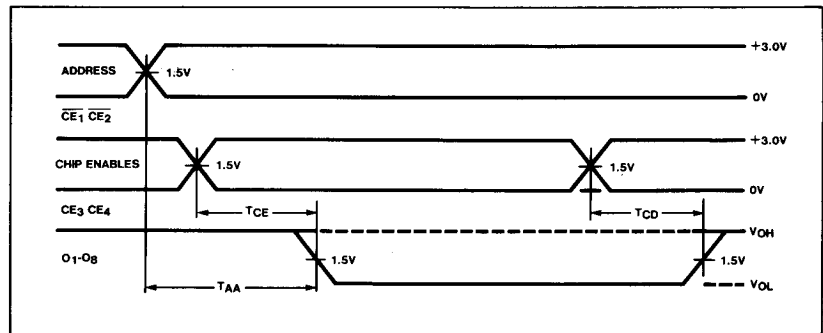
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

PROGRAMMING SYSTEM SPECIFICATIONS⁴ (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CCP} Power supply voltage To program ¹	$I_{CCP} = 425 \pm 75\text{mA}$, Transient or steady state	8.5		9.0	V
V_{CCVH} V_{CCVL} Verify limit Upper Lower		5.3 4.3		5.7 4.7	V
V_S I_{CCP} Verify threshold ² Programming supply current	$V_{CCP} = +8.75 \pm .25\text{V}$	1.4 350		1.6 500	V mA
V_{IH} V_{IL} Input voltage High Low		2.4 0		5.5 0.8	V
I_{IH} I_{IL} Input current High Low	$V_{IH} = +5.5\text{V}$ $V_{IL} = +0.4\text{V}$			50 -500	μA
V_{OPF} I_{OPF} Forced output voltage ³ (program) Forced output current (program)	$I_{OPF} = 200 \pm 20\text{mA}$, Transient or steady state $V_{OPF} = +17 \pm 1\text{V}$	16.0 180		18.0 220	V mA
T_R t_p t_D t_V Output pulse rise time $\overline{\text{CE}}$ programming pulse width Pulse sequence delay $\overline{\text{CE}}$ verify pulse width		10 100 5 1			μs μs μs μs
T_{PVA} T_{PVM} Address program verify cycle Memory program verify time (continuous)				1 20	ms sec
F_L Fusing attempts per link				1	cycle

NOTES

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle.

For a transient current of 150mA, limit voltage spikes to a maximum slew rate of $2\text{V}/\mu\text{s}$, and $10\mu\text{s}$ maximum recovery.

4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10k\Omega$ resistor to V_{CC} . Apply $\overline{CE}_1 = \text{Low}$, $\overline{CE}_2 = \text{High}$, $CE_3 = \text{High}$, $CE_4 = \text{High}$.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} .
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.

4. After t_D delay, pulse the \overline{CE}_2 input to logic low for a time t_p .
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay, lower V_{CC} to V_{CCVL} and apply a logic low level to

the \overline{CE}_2 input. All programmed outputs should remain in the logic high state.

8. After t_D delay, repeat steps 2 through 7 to program and verify all other address locations.
9. After t_D delay, raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to \overline{CE}_2 , and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE