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Memory Products	

82S183
8K-bit TTL bipolar PROM

DESCRIPTION

The 82S183 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S183 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the output drivers are controlled solely by $\overline{CE}1$, $\overline{CE}2$, and CE3 lines

A D-type latch is used to enable the 3-State output drivers. In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of Address or Chip Enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Ordering information can be found on the following page.

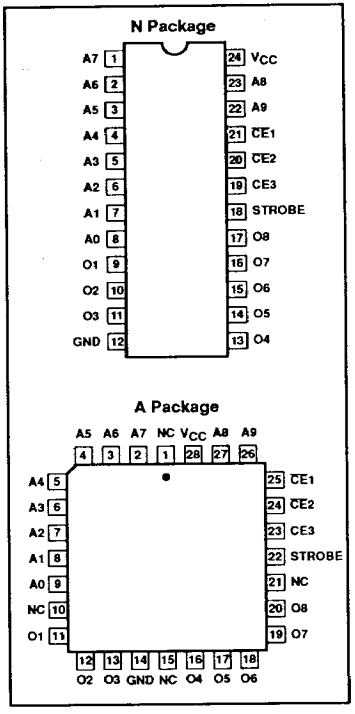
FEATURES

- Address access time: 60ns max
- Power dissipation: 80μW/bit typ
- Input loading: −100μA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Three Chip Enable inputs
- Outputs: 3-State

APPLICATIONS

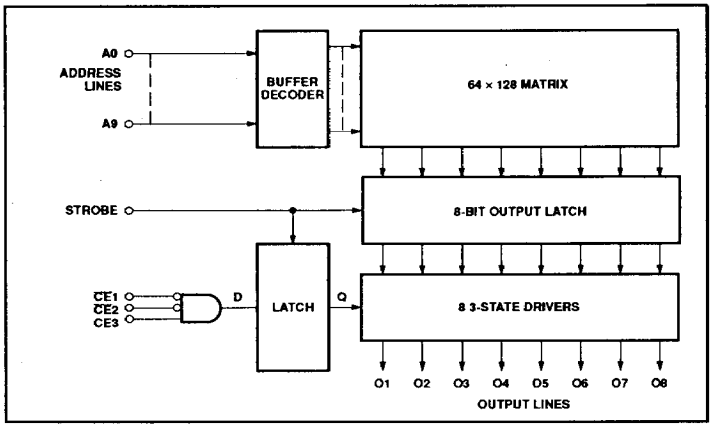
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Code conversion

PIN CONFIGURATIONS



8K-bit TTL bipolar PROM (1024 × 8) — 82S183

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 600mil-wide	N82S183 N
28-Pin Plastic Leaded Chip Carrier 450mil-square	N82S183 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[2]						
		$\overline{CE}$1,2 = Low, CE3 = High				
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	V
V_{OH}	High	I_{OUT} = -2.0mA	2.4			V
Input current[1]						
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V	25		25	µA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}$ = High, CE = Low, V_{OUT} = 5.5V			40	µA
		$\overline{CE}$ = High, CE = Low, V_{OUT} = 0.5V			-40	µA
I_{OS}	Short circuit[4]	$\overline{CE}$ = Low, CE = High, V_{OUT} = 0V High stored	-15		-70	mA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V		130	175	mA
Capacitance						
		$\overline{CE}$1,2 = High, CE3 = Low, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5V, T_{amb} = +25°C.
3. No more than one output should be grounded at the same time and Strobe should be disabled. Strobe is in High state.
4. Measured with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS

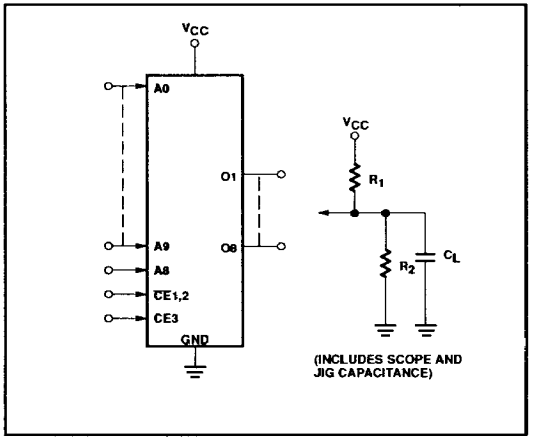
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
Access time[1]								
t_{AA}		Output	Address	Latched or transparent read		45	60	ns
t_{CE}		Output	Chip Enable			25	40	ns
Disable time[1,4]								
t_{CD}		Output	Chip Disable	Latched or transparent read		25	40	ns
Setup and hold time[3]								
t_{CDS}	Setup time	Output	Chip Enable	Latched read only	40			ns
t_{CDH}	Hold time	Output	Chip Enable		10			ns
t_{ADH}	Hold time	Output	Address	Latched or transparent read	0			ns
Pulse width[3]								
t_{SW}	Strobe			Latched read only	30	15		ns
Latch time[3]								
t_{SL}	Strobe			Latched read only	60	35		ns
Delatch time[3,4]								
t_{DL}	Strobe			Latched read only			30	ns

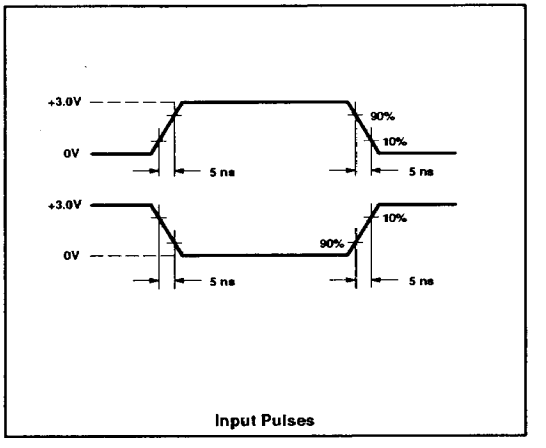
NOTES:

1. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear t_{AA} nanoseconds after the address has changed t_{CE} nanoseconds after the output circuit is enabled. t_{CD} is the time required to disable the output and switch it to an off or High impedance state after is has been enabled.
2. Typical values are $V_{CC} = 5V$, $T_{amb} = +25°C$.
3. In latched Read Mode data from any selected address will be held on the output when Strobe is lowered. Only when Strobe is raised will new location data be transferred and Chip Enable conditions be stored. The new data will appear on the output if the Chip Enable conditions enable the outputs.
4. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
5. All AC parameters are measured at 1.5V unless otherwise specified.

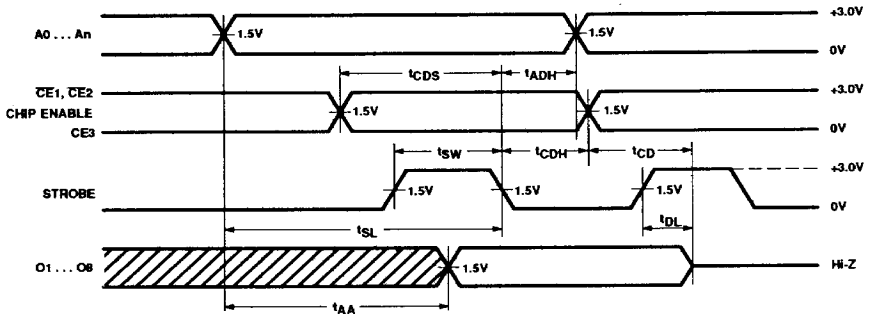
TEST LOAD CIRCUIT



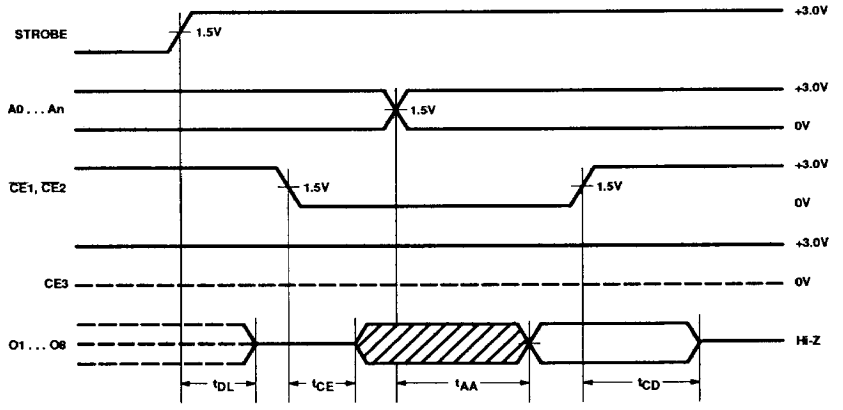
VOLTAGE WAVEFORM



TIMING DIAGRAMS[1]



Transparent Read (Output Latches Not Used)



Latched Read[2,3] (Output Latches Used)

NOTES:

1. All AC parameters are measured at 1.5V unless otherwise specified.
2. In Latched Read Mode data from any selected address will be held on the output when Strobe is lowered. Only when Strobe is raised will new location data be transferred and Chip Enable conditions be stored. The new data will appear on the output if the Chip Enable conditions enable the outputs.
3. Areas shown by crosshatch are latched data from previous address.