

Document No.	853-0131
ECN No.	86487
Date of Issue	November 11, 1986
Status	Product Specification
Memory Products	

82S185

8K-bit TTL bipolar PROM

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and one Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

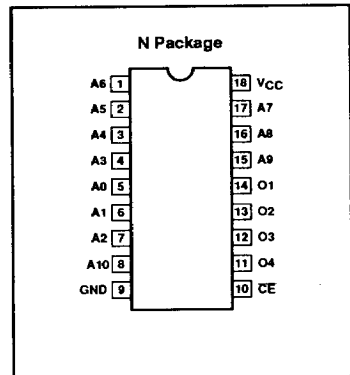
FEATURES

- Low power dissipation: 50μW/bit typ
- Address access time: 100ns max
- Input loading: -100μA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One Chip Enable input
- Outputs: 3-State

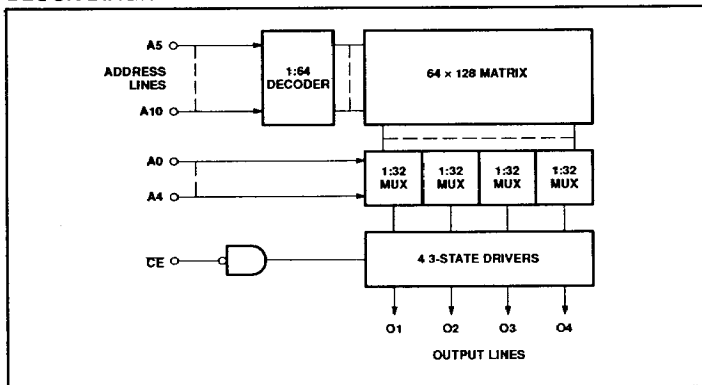
APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



8K-bit TTL bipolar PROM (2048 × 4)**82S185****ORDERING INFORMATION**

DESCRIPTION	ORDER CODE
18-Pin Plastic Dual-In-Line 300mil-wide	N82S185 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{sig}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_{amb} \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
			Min	Typ ³	Max	
Input voltage¹						
V_{IL}	Low	$I_{IN} = -12\text{mA}$	2.0		0.8	V
V_{IH}	High					
V_{IC}	Clamp					
Output voltage¹						
V_{OL}	Low	$CE = \text{Low}$ $I_{OUT} = 16\text{mA}$	2.4		0.45	V
V_{OH}	High	$I_{OUT} = -2\text{mA}$				
Input current²						
I_{IL}	Low	$V_{IN} = 0.45\text{V}$			-100	μA
I_{IH}	High	$V_{IN} = 5.5\text{V}$				
Output current						
I_{OZ}	Hi-Z state	$CE = \text{High}, V_{OUT} = 0.5\text{V}$	-15		-40	μA
I_{OS}	Short circuit ⁴	$CE = \text{High}, V_{OUT} = 5.5\text{V}$				
		$CE = \text{Low}, V_{OUT} = 0\text{V}, \text{High stored}$				40
Supply current⁵						
I_{CC}		$V_{CC} = 5.25\text{V}$		90	120	mA
Capacitance						
C_{IN}	Input	$CE = \text{High}, V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0\text{V}$		8		pF

NOTES:

- All voltage values are with respect to network ground terminal.
- Positive current is defined as into the terminal referenced.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = +25^{\circ}\text{C}$.
- Duration of short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

8K-bit TTL bipolar PROM (2048 × 4)

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AC ELECTRICAL CHARACTERISTICS

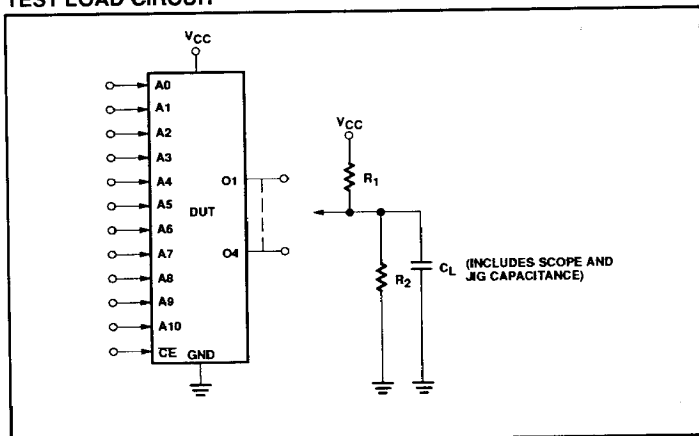
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0^\circ C \leq T_{amb} \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ¹	Max	
Access time²							
t_{AA}		Output	Address		70	100	ns
t_{CE}		Output	Chip Enable		30	40	ns
Disable time³							
t_{CD}		Output	Chip Disable		30	40	ns

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25^\circ C$.
2. Tested at an address cycle time of $1\mu s$.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS

