

# Am31L01/31L01A

64-Bit Low Power Write Transparent, Inverting Output, Bipolar RAM

Am31L01/31L01A

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## DISTINCTIVE CHARACTERISTICS

- Standard version: Address access time 50 ns
- Low power:  $I_{CC}$  typically 75 mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- High speed
- Fully decoded 16-word x 4-bit Schottky RAMs

## GENERAL DESCRIPTION

The Am31L01/31L01A is comprised of 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active-LOW chip select ( $\overline{CS}$ ) input and open-collector OR tieable outputs.

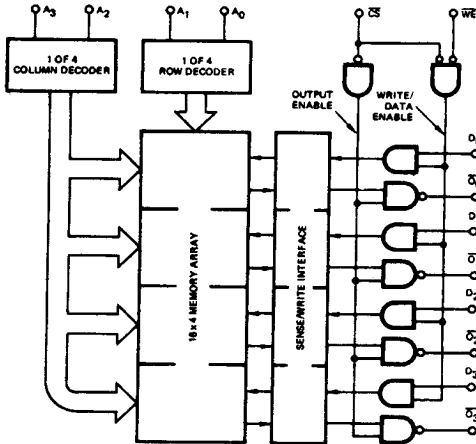
lines are LOW, the information on the four data inputs,  $D_0$  to  $D_3$ , is written into the addressed memory word. During the write cycle, the outputs are active and invert the four data inputs,  $D_0$  to  $D_3$ .

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs  $\overline{O}_0$  to  $\overline{O}_3$ .

An active-LOW Write line ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip select and write

lines are HIGH, the four outputs of the memory go to an inactive high-impedance state.

## BLOCK DIAGRAM



BD000761

## MODE SELECT TABLE

Input		Data Output Status $\overline{O}_0 - \overline{O}_3$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Data In (inverted)	Write
L	H	Selected Word (inverted)	Read
H	X	Output Disabled	Deselect

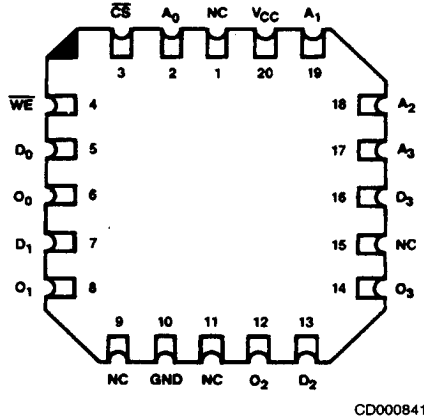
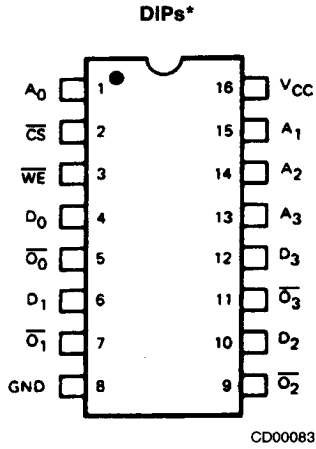
H = HIGH L = LOW X = Don't Care

## PRODUCT SELECTOR GUIDE

Open Collector (Write Transparent)	Am31L01A	Am31L01A	Am31L01	Am31L01
Access Time	55 ns	65 ns	80 ns	90 ns
$I_{CC}$	35 mA	38 mA	35 mA	38 mA
Temperature Range	C	M	C	M

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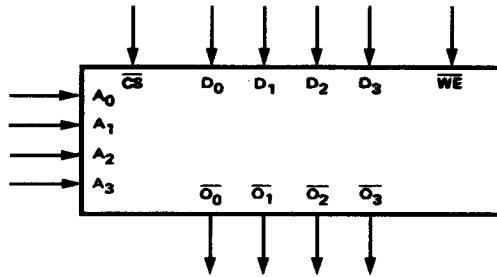
## CONNECTION DIAGRAMS Top View



\*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



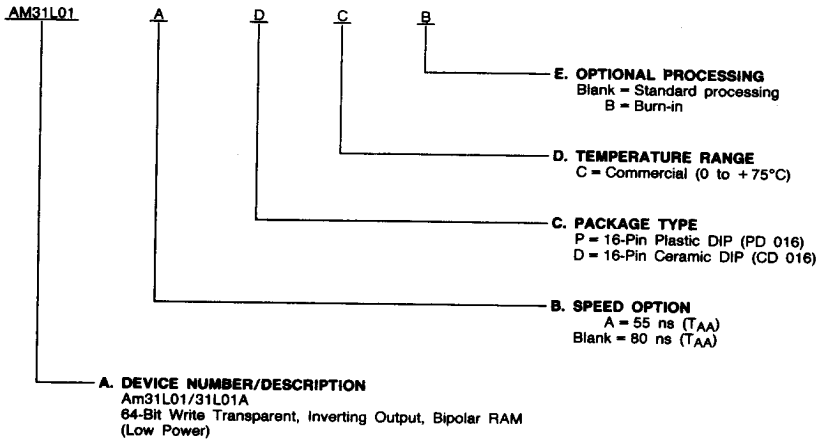
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## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations	
AM31L01	PC, PCB,
AM31L01A	DC, DCB

#### Valid Combinations

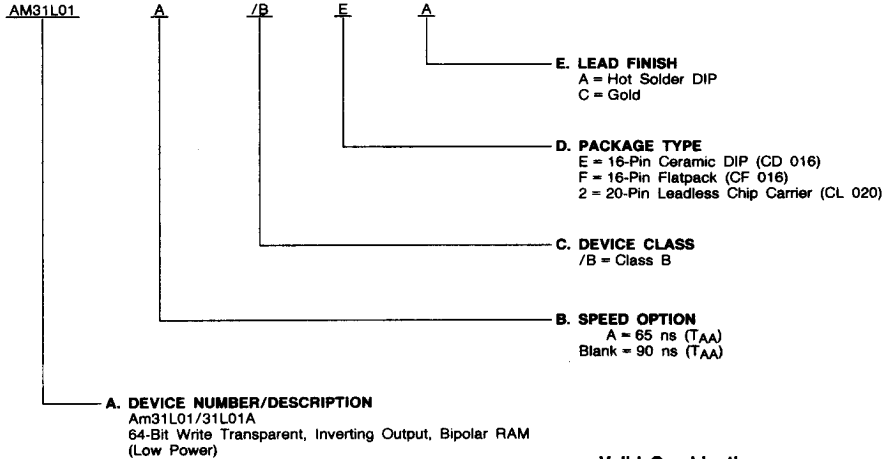
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

# ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM31L01	/BEA, /BFA,
AM31L01A	/B2C

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 8) .....	-0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State .....	-0.5 V to $V_{CC}$ Max.
DC Input Voltage .....	-0.5 V to +5.5 V
Output Current, into Outputs .....	20 mA
DC Input Current .....	-30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES (Note 3)

Commercial (C) Devices	
Temperature .....	0 to +75°C
Supply Voltage .....	+4.75 V to +5.25 V
Military (M) Devices	
Temperature .....	-55 to +125°C
Supply Voltage .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified\*

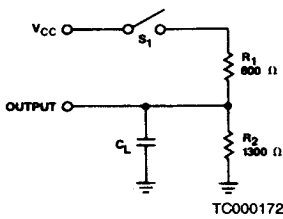
Parameter Symbol	Parameter Description	Test Conditions	Am31L01/31L01A			Units
			Min.	Typ.	Max.	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH}$ or $V_{IL}$		280	450	mV
		$I_{OL} = 8 \text{ mA}$ $I_{OL} = \text{mA}$		310	500	
$V_{IH}$	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	COM'L MIL.	2.0 2.1		Volts
$V_{IL}$	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)	COM'L MIL.		0.8 0.8	
$I_{IL}$	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = 0.40 \text{ V}$	WE, D <sub>0</sub> -D <sub>3</sub> , A <sub>0</sub> -A <sub>3</sub> CS		-30 -250	$\mu\text{A}$
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 2.7 \text{ V}$			-30 10	
$I_{CC}$	Power Supply Current	All inputs = GND $V_{CC} = \text{Max.}$	COM'L		25 35	mA
			MIL.		25 38	
$V_{CL}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$			-0.85 -1.2	Volts
$I_{CEX}$	Output Leakage Current	$V_{CS} = V_{IH}$ or $V_{WE} = V_{IL}$ $V_{OUT} = 2.4 \text{ V}, V_{CC} = \text{Max.}$			0 40	$\mu\text{A}$

- Notes: 1. Typical limits are at  $V_{CC} = 5.0 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .  
 2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.  
 3. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where  $T_A = T_C = T_J$ .  
 $\theta_{JA} \approx 50^\circ\text{C/W}$  (with moving air) for Ceramic DIP.  
 $\theta_{JC} \approx 10\text{--}17^\circ\text{C/W}$  for Flatpack and Leadless Chip Carrier.

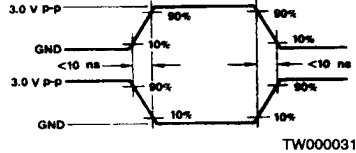
\*See the last page of this spec for Group A Subgroup Testing information.

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### SWITCHING TEST CIRCUIT



### SWITCHING TEST WAVEFORM



### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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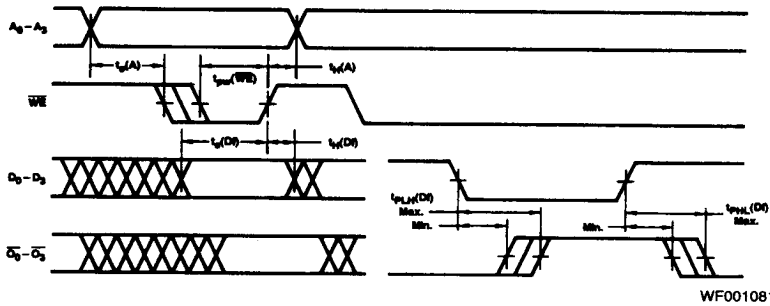
### SWITCHING CHARACTERISTICS over operating range unless otherwise specified\*

No.	Parameter Symbol	Parameter Description	Am31L01A				AM31L01				Units
			C Devices		M Devices		C Devices		M Devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	$t_{PLH}(A)$	Delay from Address to Output		55		65		80		90	ns
2	$t_{PHL}(A)$										
3	$t_{pZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		30		35		60		70	ns
4	$t_{pZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery - See Note 1)		30		35		80		100	ns
5	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
6	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		0		0		ns
7	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	45		55		60		80		ns
8	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
9	$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	45		55		60		80		ns
10	$t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)		30		35		50		60	ns
11	$t_{PLH}(DI)$	Delay from Data Input to Correct Data Output ( $\overline{WE} = \overline{CS} = V_{IL}$ )		55		65		80		90	ns
12	$t_{PHL}(DI)$										

- Notes: 1. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs during write and after write is terminated. (No write recovery glitch).  
 2.  $t_{PLH}(A)$  and  $t_{PHL}(A)$  are tested with  $S_1$  closed and  $C_L = 30$  pF with both input and output timing referenced to 1.5 V.  
 3. All delays from Write Enable ( $\overline{WE}$ ) or Chip Select ( $\overline{CS}$ ) inputs to the Data Output (DO<sub>UT</sub>),  $t_{PLZ}(\overline{WE})$ ,  $t_{PLZ}(\overline{CS})$ ,  $t_{pZL}(\overline{WE})$  and  $t_{pZL}(\overline{CS})$  are measured with  $S_1$  closed and  $C_L = 30$  pF and with both the input and output timing referenced to 1.5 V.

\*See the last page of this spec for Group A Subgroup Testing information.

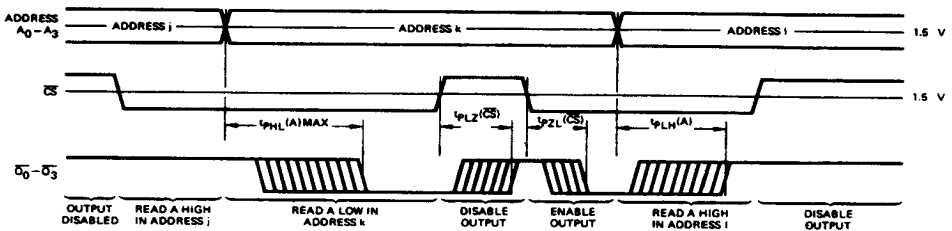
## SWITCHING WAVEFORMS



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### Write Mode

**Write Cycle Timing.** The cycle is initiated by an address change. After  $t_g(A)$  Min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse,  $t_h(A)$  Min. must be allowed before the address may be changed again. The output will be the complement of the data input while the write enable ( $WE$ ) is LOW.



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### Read Mode

Switching delays from address and chip select inputs to the data output.

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## GROUP A SUBGROUP TESTING

### DC CHARACTERISTICS

Parameter Symbol	Subgroups
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub>	1, 2, 3
I <sub>IL</sub>	1, 2, 3
I <sub>IH</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
V <sub>CL</sub>	1, 2, 3
I <sub>CEX</sub>	1, 2, 3

### SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t <sub>PLH</sub> (A)	9, 10, 11
2	t <sub>PHL</sub> (A)	9, 10, 11
3	t <sub>PZL</sub> ( $\overline{CS}$ )	9, 10, 11
4	t <sub>PZL</sub> ( $\overline{WE}$ )	9, 10, 11
5	t <sub>s</sub> (A)	9, 10, 11
6	t <sub>h</sub> (A)	9, 10, 11
7	t <sub>s</sub> (DI)	9, 10, 11
8	t <sub>h</sub> (DI)	9, 10, 11
9	t <sub>pw</sub> ( $\overline{WE}$ )	9, 10, 11
10	t <sub>PLZ</sub> ( $\overline{CS}$ )	9, 10, 11
11	t <sub>PLH</sub> (DI)	9, 10, 11
12	t <sub>PHL</sub> (DI)	9, 10, 11

### MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.