DALLAS SEMICONDUCTOR

Application Note 93
Design Guidelines for Microcontrollers Incorporating NVRAM

OVERVIEW

Microcontrollers which incorporates battery-backed, nonvolatile SRAM (NVRAM) have found wide acceptance in the embedded marketplace. Unlike Flash memory or EEPROM technology, nonvolatile SRAM has no write limitations, which makes it ideal for real-time data logging applications. In products such as the Dallas Semiconductor Secure Microcontroller family, NVRAM can be used to provide in-system reprogrammable program memory.

This application note discusses design guidelines for microcontroller products which incorporate NVRAM. A number of design suggestions are presented to improve the reliability of microcontrollers which incorporate NVRAM. It should be stressed that battery-backed memory is as reliable as nonvolatile memory as long as standard CMOS design guidelines are used. This application note is applicable to the Secure Microcontroller family of products (DS5000, DS5001FP, DS5002FP, DS2250(T), DS2251T, DS2252T) as well as the DS87C530 High-Speed Microcontroller.

OUT-OF-TOLERANCE VOLTAGE SPIKES

The"real world" is a harsh place; electrostatic discharge (ESD), electrical noise, etc., can enter into a system. Many of these phenomena can induce negative voltages on one or more device pins.CMOS design guidelines require that no pin be taken above V_{CC} or below V_{SS}. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents).

Negative voltage spikes are a particular problem for CMOS devices. When a negative voltage spike is experienced, one or more parasitic diodes inside the device can become forward-biased. This will cause the device to consume a large amount of current, and can cause the device to latch-up. In general, the only way to reverse CMOS latch-up is to remove power from the device. If the supply to the device is not limited, the excessive current draw can cause irreparable damage to the device.

Less severe, but just as troublesome, is the effect this can have on nonvolatile memory. When a parasitic diode forms, a high-current path will form. This will drain current away from the device, and may cause the voltage to sag internally. If the internal voltage drops below the minimum needed to maintain the memory, soft errors may be experienced.

In a practical application, it is often difficult or impossible to remove all voltages above V_{CC} or below V_{SS}. Realistically, overshoots or undershoots of 0.3 V can be tolerated by most devices. The following cases discuss common causes of such conditions and ways to minimize their effect on systems.

PROTECTING I/O PINS

The most common way that a device experiences negative voltage spikes is through its general-purpose I/O pins. These are usually the only contact that the microcontroller has with the "outside world." Devices such as electrical motors and keypads can generate large amounts of electrical noise. The shock that one experiences when touching a doorknob, for example, can be as much as 30 kV. If this voltage is transmitted from a keypad into a microcontroller system, it can seriously damage electronic components.

Figure 1 demonstrates a diode protection scheme that can be used to protect the I/O pins of a microcontroller. The scheme relies on the use of Schottky diode and current limiting resistor to reduce the effect of current spikes on the device. When the voltage approaching the device pin exceeds V_{CC} or V_{SS} by more than 0.1V – 0.2V, the Schottky diodes will become forward biased, conducting the excess voltage away from the device pins. The current limiting resistors will also help dampen the effect of the voltage spike on the microcontroller.