

1103

1024x1 DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION - The 1103 is a fully decoded 1024-word by 1-bit Dynamic Random Access Memory, especially suited for main memory applications. The circuitry is designed for maximum speed and low standby power dissipation. It requires two power supplies and two clocks including the Chip Enable (CE). Readout is non-destructive and the Data Out can be wired-OR for ease of expansion. Exercise of the 32 row addresses is required for refresh.

The 1103 is manufactured with the p-channel Isoplanar process. It is available in 18-pin ceramic Dual In-line Packages in the commercial temperature range.

- FAST ACCESS (120, 150, 220 AND 300 ns)
- LOW POWER
- FULLY EXPANDABLE
- FULLY DECODED
- WIRED-OR CAPABILITY
- 18-PIN CERAMIC DUAL IN-LINE PACKAGE

PIN NAMES

A _n	Address Inputs
D _{IN}	Data Input
D _{OUT}	Data Output
CE	Chip Enable
R/W	Read/Write
P	Precharge

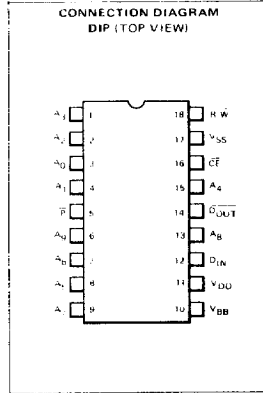
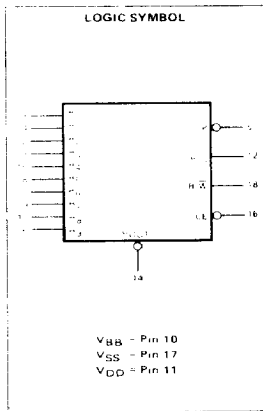
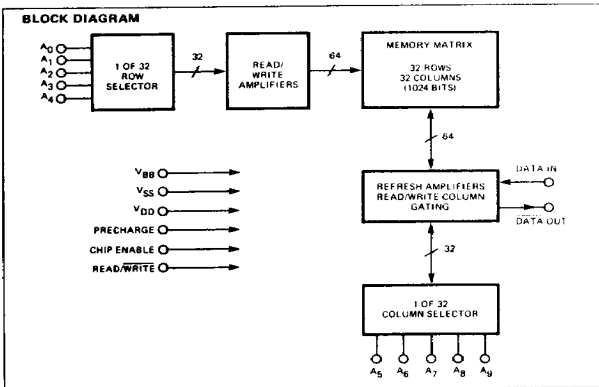
ABSOLUTE MAXIMUM RATINGS

All Pins with Respect to V_{BB}

Storage Temperature

Operating Temperature: 1103-1, 1103S, 1103F
1103

-25 V to +0.3 V
-55 C to +150 C
0 C to +55 C
0 C to +70 C



FAIRCHILD MOS INTEGRATED CIRCUITS • 1103

DC REQUIREMENTS: 1103F, T_A = 0°C to +55°C, 1103, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V _{SS}	Positive Supply Voltage	18	20	15.2	16.8	V	
V _{BB}	Bias Supply Voltage	V _{SS} +3	V _{SS} +4	V _{SS} +3	V _{SS} +4	V	
V _{DD}	Negative Supply Voltage	0	0	0	0	V	
V _{IH1}	Input HIGH Voltage	V _{SS} -1	V _{SS} +1	V _{SS} -1	V _{SS} +1	V	T _A = Min
V _{IH2}	Input HIGH Voltage	V _{SS} -1	V _{SS} +1	V _{SS} -0.7	V _{SS} +1	V	T _A = Max
V _{IL1*}	Input LOW Voltage (A)	V _{SS} -20	V _{SS} -18	V _{SS} -17	V _{SS} -14.2	V	T _A = Min
V _{IL2*}	Input LOW Voltage (A)	V _{SS} -20	V _{SS} -18	V _{SS} -17	V _{SS} -14.5	V	T _A = Max
V _{IL3*}	Input LOW Voltage (B)	V _{SS} -20	V _{SS} -18	V _{SS} -17	V _{SS} -14.7	V	T _A = Min
V _{IL4*}	Input LOW Voltage (B)	V _{SS} -20	V _{SS} -18	V _{SS} -17	V _{SS} -15	V	T _A = Max

* See waveforms input type

DC CHARACTERISTICS: 1103F, T_A = 0°C to +55°C, 1103, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V _{OH1}	Output HIGH Voltage	115	700	60	400	mV	T _A = 25°C, Note 1
V _{OH2}	Output HIGH Voltage	90	700	50	400	mV	T _A = Max Operating Temperature, Note 1
V _{OL}	Output LOW Voltage						Note 2
I _{OH1}	Output HIGH Current	1150	7000	600	4000	μA	T _A = 25°C
I _{OH2}	Output HIGH Current	900	7000	500	4000	μA	T _A = Max Operating Temperature
I _{OL}	Output LOW Current						Note 2
I _{IN}	Input Load Current		10		1.0	μA	
I _{OUT}	Output Leakage Current		10		1.0	μA	
I _{BB}	V _{BB} Supply Current		100		100	μA	
I _{DD1}	Supply Current During t _{PC}		60		56	mA	
I _{DD2}	Supply Current During t _{OV}		68.5		59	mA	T _A = 25°C
I _{DD3}	Supply Current During t _{POV}		11		11	mA	
I _{DD4}	Supply Current During t _{CP}		4.0		4.0	mA	
I _{DDAV}	Average Supply Current		26		25	mA	T _A = 25°C, Note 3

1. Assumes a load resistor of 100 Ω.
2. The output current and voltage for LOW is a function of load resistor.
3. t_{AWC} = min. Precharge width at 50%: 1103F, 60 ns, 1103, 190 ns.

AC REQUIREMENTS: 1103F, T_A = 0°C to +55°C, 1103, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t _{REF}	Time Between Refresh		2.0		2.0	ns	
t _{AC}	Address to Chip Enable Set-up Time	30		115		ns	
t _{CA}	Chip Enable to Address Hold Time	10		20		ns	
t _{PC}	Precharge to Chip Enable Delay	35		125		ns	
t _{CP}	Chip Enable to Precharge Delay	40		95		ns	
t _{OV_L}	Precharge and Chip Enable Overlap LOW			25	75	ns	
t _{OV_H}	Precharge and Chip Enable Overlap HIGH				140	ns	
t _{QVM}	Precharge and Chip Enable Overlap, 50% Points	13	50	45	95	ns	
t _{RC}	Read Cycle	238		480		ns	Note 4
t _{POV}	Precharge to End Chip Enable (Read Cycle)	114	700	165	500	ns	
t _{WC}	Write Cycle	270		580		ns	Note 4
t _{RWC}	Read/Write Cycle	270		580		ns	Note 4
t _{PW}	Precharge to Read/Write Delay	114	700	165	500	ns	
t _{WP}	Read/Write Pulse Width	20		50		ns	
t _W	Read/Write Set-up Time	20		80		ns	
t _{DW}	Data Set-up Time	25		105		ns	
t _{DH}	Data Hold Time	10		10		ns	
t _{CW}	Relationship between Chip Enable and Read/Write		5.0		0	ns	

4. Assumes t_r = 12 ns for 1103F, 20 ns for 1103.

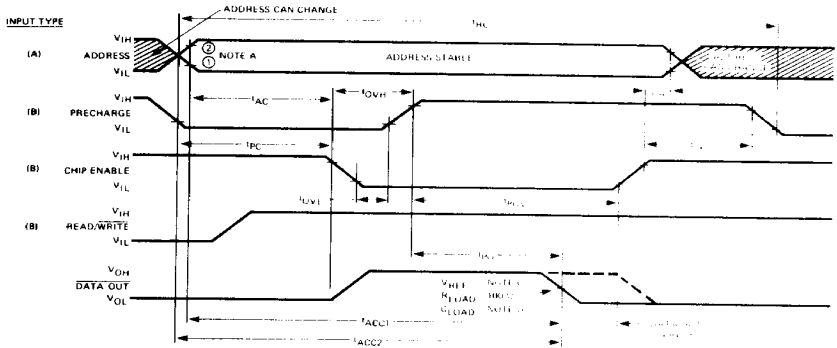
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AC CHARACTERISTICS: 1103F, T_A = 0° C to 55° C; 1103, T_A = 0° C to +70° C

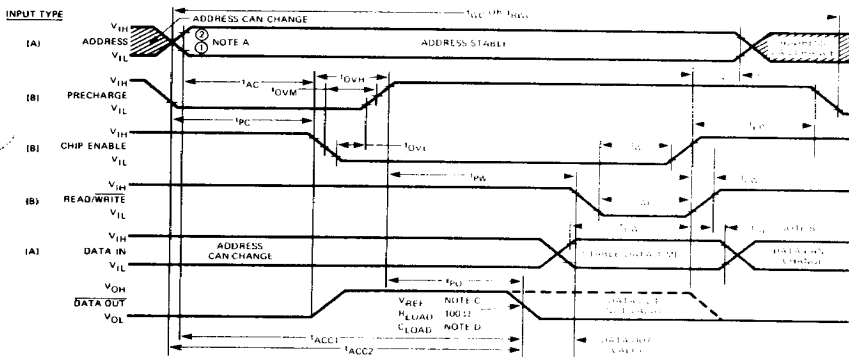
SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t _{PD}	End of Precharge to Output Delay (See Waveforms)		65		120	ns	
t _{ACC1}	Address to Output Access		120		300	ns	Note 5
t _{ACC2}	Precharge to Output Access		125		310	ns	Note 6

5. t_{ACC1}(max) = t_{AC} min + t_{OVL} min + t_{PO} max + 2t₁
 6. t_{ACC2}(max) = t_{PC} min + t_{OVL} min + t_{PO} max + 2t₁

**WAVEFORMS
READ CYCLE**



WRITE CYCLE OR READ/WRITE CYCLE



NOTES:

A. Point ① = V_{DD} + 2.0 V }
 Point ② = V_{SS} - 2.0 V } t₁ is defined as the transitions between these two points

B. t_{PH} is referenced to point ② of the rising edge of Chip Enable or Read/Write, whichever occurs first.

C. V_{REF} = 80 mV (1103F, 1103-1), 40 mV (1103, 1103S)

D. C_{LOAD} = 50 pF (1103F, 1103-1), 100 pF (1103, 1103S)

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Source New F

DC REQUIREMENTS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V _{SS}	Positive Supply Voltage	18.05	19.95	18.05	19.95	V	
V _{BB}	Bias Supply Voltage	V _{SS} +3	V _{SS} +4	V _{SS} +3	V _{SS} +4	V	
V _{DD}	Negative Supply Voltage	0	0	0	0	V	
V _{IH1}	Input HIGH Voltage	V _{SS} -1	V _{SS} +1	V _{SS} -1	V _{SS} +1	V	T _A = 0°C
V _{IH2}	Input HIGH Voltage	V _{SS} -1	V _{SS} +1	V _{SS} -0.7	V _{SS} +1	V	T _A = 55°C
V _{IL1*}	Input LOW Voltage (A)	V _{SS} -20	V _{SS} -18	V _{SS} -20	V _{SS} -17	V	T _A = 0°C
V _{IL2*}	Input LOW Voltage (A)	V _{SS} -20	V _{SS} -18	V _{SS} -20	V _{SS} -17.3	V	T _A = 55°C
V _{IL3*}	Input LOW Voltage (B)	V _{SS} -20	V _{SS} -18	V _{SS} -20	V _{SS} -17	V	T _A = 0°C
V _{IL4*}	Input LOW Voltage (B)	V _{SS} -20	V _{SS} -18	V _{SS} -20	V _{SS} -17.3	V	T _A = 55°C

* See waveforms input type.

DC CHARACTERISTICS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V _{OH1}	Output HIGH Voltage	115	700	60	700	mV	T _A = +25°C, Note 1
V _{OH2}	Output HIGH Voltage	90	700	50	700	mV	T _A = 55°C, Note 1
V _{OL}	Output LOW Voltage						Note 2
I _{OH1}	Output HIGH Current	1150	7000	600	7000	μA	T _A = 25°C
I _{OH2}	Output HIGH Current	900	7000	500	7000	μA	T _A = 55°C
I _{OL}	Output LOW Current						Note 2
I _{LI}	Input Load Current		10		10	μA	
I _{LO}	Output Leakage Current		10		10	μA	
I _{BB}	V _{BB} Supply Current		100		100	μA	
I _{DD1}	Supply Current During t _{PC}		60		60	mA	
I _{DD2}	Supply Current During t _{QV}		68.5		68.5	mA	T _A = 25°C
I _{DD3}	Supply Current During t _{QOV}		11		11	mA	
I _{DD4}	Supply Current During t _{CP}		4.0		4.0	mA	
I _{DDAV}	Average Supply Current		26		24	mA	T _A = 25°C, Note 7

7. t_{RWC} = min; Precharge width at 50%: 1103-1, 105 ns; 1103S, 95 ns.

AC REQUIREMENTS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS	
		MIN	MAX	MIN	MAX			
t _{REF}	Time Between Refresh		1.0		1.0	ms		
t _{AC}	Address to Chip Enable Set-up Time		30		70	ns		
t _{CA}	Chip Enable to Address Hold Time		10		20	ns		
t _{PC}	Precharge to Chip Enable Delay		60		70	ns		
t _{CP}	Chip Enable to Precharge Delay		40		50	ns		
t _{QVL}	Precharge and Chip Enable Overlap LOW		5.0	30	5.0	45	ns	
t _{QVH}	Precharge and Chip Enable Overlap HIGH			85		105	ns	
t _{QVM}	Precharge and Chip Enable Overlap, 50% Points		25	50		ns		
t _{RC}	Read Cycle		300		345	ns	t _T = 20 ns	
t _{POV}	Precharge to End Chip Enable (Read Cycle)		115	500	140	500	ns	
t _{WC}	Write Cycle		340		390	ns	t _T = 20 ns	
t _{RWC}	Read/Write Cycle		340		390	ns	t _T = 20 ns	
t _{WP}	Precharge to Read/Write Delay		115	500	140	500	ns	
t _{WP}	Read/Write Pulse Width		20		25	ns		
t _W	Read/Write Set-up Time		20		25	ns		
t _{DW}	Data Set-up Time		40		45	ns		
t _{DH}	Data Hold Time		10		10	ns		
t _{CV}	Relationship between Chip Enable and Read/Write			0		ns		

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AC CHARACTERISTICS: 1103-1 and 1103S, $T_A = 0^\circ\text{C}$ to $+55^\circ\text{C}$

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{PO}	End of Precharge to Output Delay (See Waveforms)		75		105	ns	
t_{ACC1}	Address to Output Access		150		220	ns	Note 5
t_{ACC2}	Precharge to Output Access		180		220	ns	Note 6

CAPACITANCE CHARACTERISTICS (pF): All unused pins at AC ground, $f_0 = 1\text{ MHz}$, $V_{BB} = +3.0\text{ Volts}$

SYMBOL	CAPACITANCE	1103, 1103-1, 1103S, 1103F		CONDITIONS
		TYP	MAX	
C_{AD}	Address	6.0	8.0	V_{IN} V_{SS}
C_{PR}	Precharge	19	23	V_{IN} V_{SS}
C_{CE}	Chip Enable	15	18	V_{IN} V_{SS}
C_{RW}	Read/Write	15	18	V_{IN} V_{SS}
C_{IN}	Data Input	5.0	7.0	Chip Enable V_{DD} or V_{SS} , V_{IN} V_{SS}
C_{OUT}	Data Output	3.0	4.0	V_{OUT} V_{DD}