40097B•40098B

3-STATE HEX NON-INVERTING AND INVERTING BUFFERS

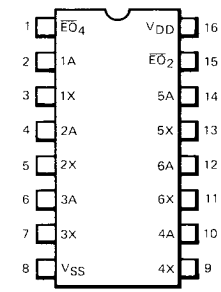
DESCRIPTION – These two CMOS buffers provide high current output capability suitable for driving high capacitance loads. The 40097B is a Non-Inverting CMOS Buffer with 3-state outputs and the 40098B is an Inverting CMOS Buffer with 3-state outputs. The 3-state outputs of each device are controlled by two Enable Inputs ($\overline{EO}_4$, $\overline{EO}_2$). A HIGH on Enable Input $\overline{EO}_4$ causes the Outputs of four of the six buffer elements to assume a high impedance or OFF state, regardless of other input conditions and a HIGH on Enable Input $\overline{EO}_2$ causes the Outputs of the remaining two buffer elements to assume a high impedance or OFF state, regardless of other input conditions.

- **3-STATE OUTPUTS**
- **TTL COMPATIBLE – FAN OUT OF ONE TTL LOAD**
- **ACTIVE LOW ENABLE INPUTS**

PIN NAMES

1A-6A	Buffer Inputs
$\overline{EO}_4$, $\overline{EO}_2$	Enable Inputs (Active LOW)
1X-6X	Buffer Outputs (Active HIGH for the 40097B and Active LOW for the 40098B)

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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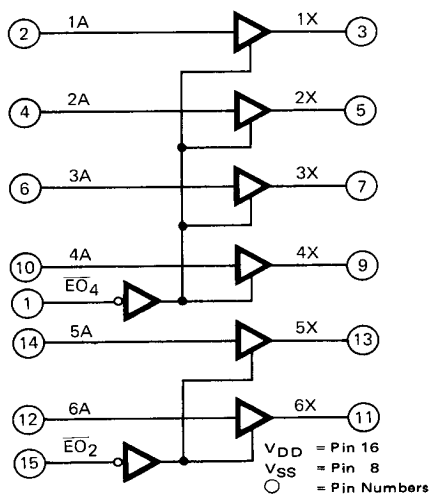
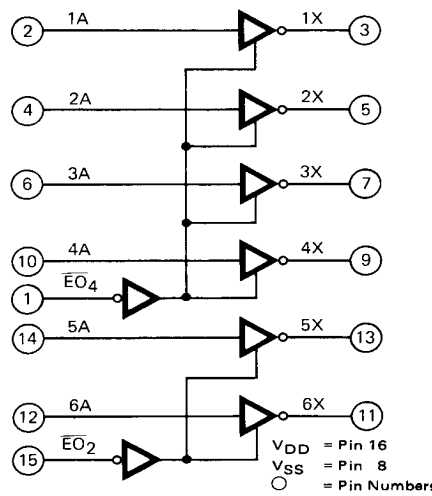
40097B LOGIC DIAGRAM



40098B LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OH}	Output HIGH Current		-1.0			-2.0			-3.2			mA	MIN, 25°C	V_{OUT} = 4.5 V for V_{DD} = 5 V V_{OUT} = 9.5 V for V_{DD} = 10 V V_{OUT} = 14.5 V for V_{DD} = 15 V Inputs at V_{SS} or V_{DD} Per Logic Function
			-0.7			-1.4			-2.2				MAX	
I_{OL}	Output LOW Current		2.5			6.25			11.25			mA	MIN, 25°C	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V V_{OUT} = 0.5 V for V_{DD} = 15 V Inputs at V_{SS} or V_{DD} Per Logic Function
			1.8			4.5			8.25				MAX	
I_{OZH}	Output OFF Current HIGH	XC									1.6	µA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}_n = V_{DD}$
											12		MAX	
		XM									0.4		MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	µA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}_n = V_{DD}$
											-12		MAX	
		XM									-0.4		MIN, 25°C	
											-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			4			8			16	µA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					30			60			120		MAX	
		XM			1			2			4		MIN, 25°C	
					30			60			120		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 40097B only (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		65	100		25	40		20	32	ns	C_L = 50 pF,
t_{PHL}	Data to Output		80	100		28	40		20	32		R_L = 200 kΩ
t_{PZH}	Output Enable Time		70	110		35	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			95	150		40	65		30	52		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		40	65		31	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			60	95		35	55		30	44		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		40	65		25	40		15	30	ns	Input Transition
t_{THL}			30	60		15	30		15	30		Times ⩽ 20 ns

Notes on following page.

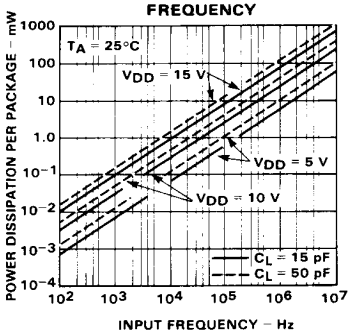
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 40098B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Data to Output		65	120		30	55		30	44	ns	C_L = 50 pF,
t_{PHL}			85	155		35	65		30	52		R_L = 200 kΩ
t_{PZH}	Output Enable Time		70	110		35	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			95	170		40	60		30	48		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Outside Disable Time		40	70		31	55		29	44	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			60	105		35	55		30	44		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		40	65		25	40		15	30	ns	Input Transition
t_{THL}			30	60		15	30		15	30		Times ⩽ 20 ns

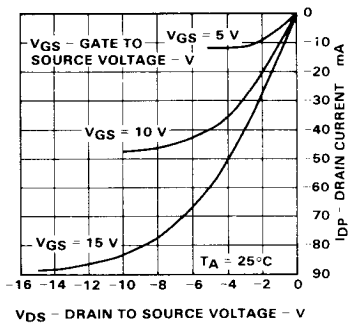
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

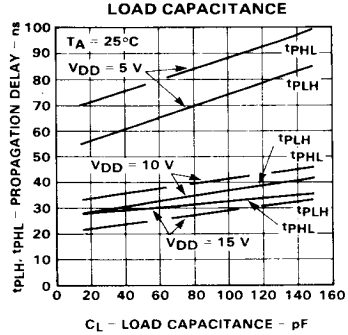
40097B/40098B
POWER DISSIPATION VERSUS FREQUENCY



40097B/40098B
P-CHANNEL DRAIN CHARACTERISTICS

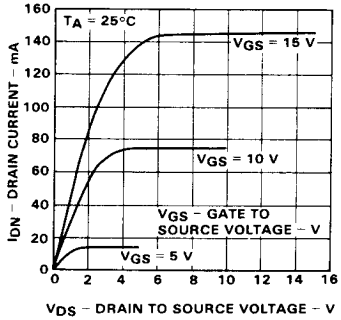


40098B
PROPAGATION DELAY VERSUS LOAD CAPACITANCE

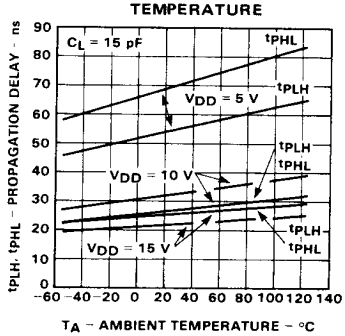


TYPICAL ELECTRICAL CHARACTERISTICS (Cont'd)

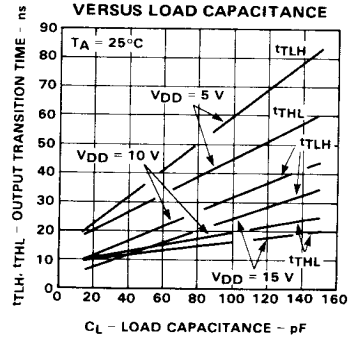
40098B
N-CHANNEL DRAIN CHARACTERISTICS



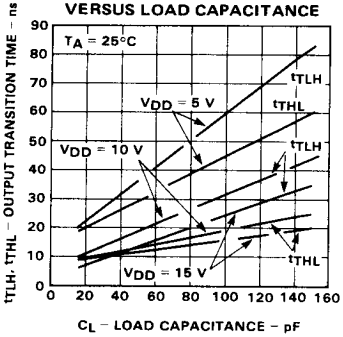
40098B
PROPAGATION DELAY VERSUS TEMPERATURE



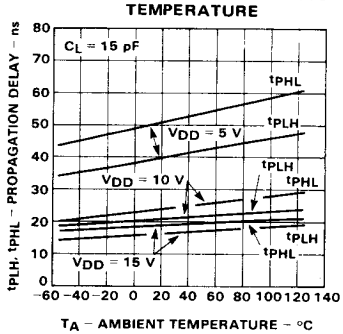
40098B
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



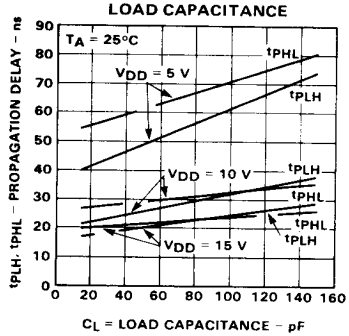
40097B
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



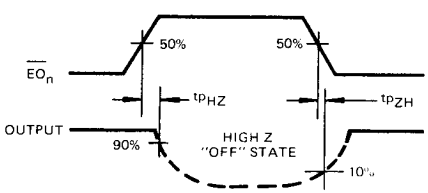
40097B
PROPAGATION DELAY VERSUS TEMPERATURE



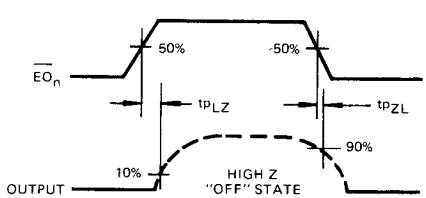
40097B
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})