

## CD4016BC Quad Bilateral Switch

### General Description

The CD4016BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4066BC.

### Features

- Wide supply voltage range: 3V to 15V
- Wide range of digital and analog switching:  $\pm 7.5 V_{PEAK}$
- "ON" resistance for 15V operation: 400 $\Omega$  (typ.)
- Matched "ON" resistance over 15V signal input:  $\Delta R_{ON} = 10\Omega$  (typ.)
- High degree of linearity:
  - 0.4% distortion (typ.)
  - @  $f_{IS} = 1$  kHz,  $V_{IS} = 5 V_{p-p}$ ,  
 $V_{DD} - V_{SS} = 10V$ ,  $R_L = 10$  k $\Omega$
- Extremely low "OFF" switch leakage:
  - 0.1 nA (typ.)
  - @  $V_{DD} - V_{SS} = 10V$
  - $T_A = 25^\circ C$

- Extremely high control input impedance:  $10^{12}\Omega$  (typ.)
- Low crosstalk between switches:
  - 50 dB (typ.)
  - @  $f_{IS} = 0.9$  MHz,  $R_L = 1$  k $\Omega$
- Frequency response, switch "ON": 40 MHz (typ.)

### Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

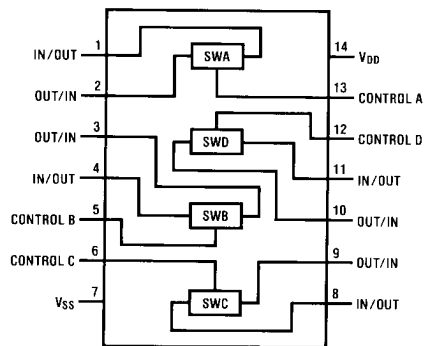
### Ordering Code:

Order Number	Package Number	Package Description
CD4016BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
CD4016BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

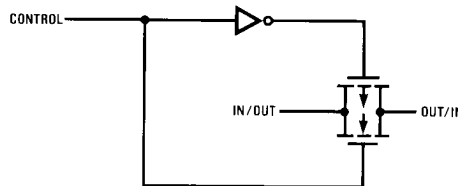
Devices also available in Tape and Reel. Specify by appending the letter suffix "X" to the ordering code.

### Connection Diagram

Pin Assignments for DIP and SOIC



### Schematic Diagram



Absolute Maximum Ratings <sup>(Note 1)</sup> (Note 2)			Recommended Operating Conditions <sup>(Note 2)</sup>							
$V_{DD}$ Supply Voltage		-0.5V to +18V	$V_{DD}$ Supply Voltage		3V to 15V					
$V_{IN}$ Input Voltage		-0.5V to $V_{DD} + 0.5V$	$V_{IN}$ Input Voltage		0V to $V_{DD}$					
$T_S$ Storage Temperature Range		-65°C to +150°C	$T_A$ Operating Temperature Range		-40°C to +85°C					
Power Dissipation ( $P_D$ )			<b>Note 1:</b> "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.							
Dual-In-Line		700 mW	<b>Note 2:</b> $V_{SS} = 0V$ unless otherwise specified.							
Small Outline		500 mW								
Lead Temperature (Soldering, 10 seconds)		260°C								
DC Electrical Characteristics <sup>(Note 2)</sup>										
Symbol	Parameter	Conditions	-40°C		25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		1.0		0.01	1.0		7.5	$\mu A$
	Current	$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		2.0		0.01	2.0		15	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$			4.0		0.01	4.0		30
Signal Inputs and Outputs										
$R_{ON}$	"ON" Resistance	$R_L = 10k\Omega$ to $(V_{DD} - V_{SS})/2$								
		$V_C = V_{DD}, V_{IS} = V_{SS}$ or $V_{DD}$								
		$V_{DD} = 10V$		610		275	660		840	$\Omega$
		$V_{DD} = 15V$		370		200	400		520	$\Omega$
$\Delta R_{ON}$	$\Delta$ "ON" Resistance Between any 2 of 4 Switches (In Same Package)	$R_L = 10k\Omega$ to $(V_{DD} - V_{SS})/2$								
		$V_C = V_{DD}, V_{IS} = V_{SS}$ to $V_{DD}$								
		$V_{DD} = 10V$				15				$\Omega$
		$V_{DD} = 15V$				10				$\Omega$
$I_{IS}$	Input or Output Leakage Switch "OFF"	$V_C = 0, V_{DD} = 15V$		$\pm 50$		$\pm 0.1$	$\pm 50$		$\pm 200$	nA
		$V_{IS} = 0V$ or $15V,$ $V_{OS} = 15V$ or $0V$								
Control Inputs										
$V_{ILC}$	LOW Level Input Voltage	$V_{IS} = V_{SS}$ and $V_{DD}$								
		$V_{OS} = V_{DD}$ and $V_{SS}$								
		$I_{IS} = \pm 10 \mu A$								
		$V_{DD} = 5V$		0.9			0.7		0.4	V
$V_{IHC}$	HIGH Level Input Voltage	$V_{DD} = 10V$		0.9			0.7		0.4	V
		$V_{DD} = 15V$		0.9			0.7		0.4	V
		$V_{DD} = 5V$		0.9			0.7		0.4	V
$V_{IHC}$	HIGH Level Input Voltage	$V_{DD} = 5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$	11.0		11.0			11.0		V
$I_{IN}$	Input Current	(Note 3) and Figure 8								
		$V_{CC} - V_{SS} = 15V$		$\pm 0.3$		$\pm 10^{-5}$	$\pm 0.3$		$\pm 1.0$	$\mu A$
		$V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$								
<b>Note 3:</b> If the switch input is held at $V_{DD}$ , $V_{IHC}$ is the control input level that will cause the switch output to meet the standard "B" series $V_{OH}$ and $I_{OH}$ output levels. If the analog switch input is connected to $V_{SS}$ , $V_{IHC}$ is the control input level — which allows the switch to sink standard "B" series $I_{OL}$ , high level current, and still maintain a $V_{OL} \leq$ "B" series. These currents are shown in Figure 8.										

AC Electrical Characteristics (Note 4)						
T <sub>A</sub> = 25°C, t <sub>r</sub> = t <sub>f</sub> = 20 ns and V <sub>SS</sub> = 0V unless otherwise specified						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time Signal Input to Signal Output	V <sub>C</sub> = V <sub>DD</sub> , C <sub>L</sub> = 50 pF, (Figure 1) R <sub>L</sub> = 200k V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		58 27 20	100 50 40	ns ns ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Propagation Delay Time Control Input to Signal Output HIGH Impedance to Logical Level	R <sub>L</sub> = 1.0 kΩ, C <sub>L</sub> = 50 pF, (Figure 2, Figure 3) V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		20 18 17	50 40 35	ns ns ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Propagation Delay Time Control Input to Signal Output Logical Level to HIGH Impedance Sine Wave Distortion	R <sub>L</sub> = 1.0 kΩ, C <sub>L</sub> = 50 pF, (Figure 2, Figure 3) V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V V <sub>C</sub> = V <sub>DD</sub> = 5V, V <sub>SS</sub> = -5 R <sub>L</sub> = 10 kΩ, V <sub>IS</sub> = 5 V <sub>P-P</sub> , f = 1 kHz, (Figure 4)		15 11 10 0.4	40 25 22	ns ns ns %
	Frequency Response — Switch "ON" (Frequency at -3 dB)	V <sub>C</sub> = V <sub>DD</sub> = 5V, V <sub>SS</sub> = -5V, R <sub>L</sub> = 1 kΩ, V <sub>IS</sub> = 5 V <sub>P-P</sub> , 20 Log <sub>10</sub> V <sub>OS</sub> /V <sub>OS</sub> (1 kHz) -dB, (Figure 4)		40		MHz
	Feedthrough — Switch "OFF" (Frequency at -50 dB)	V <sub>DD</sub> = 5V, V <sub>C</sub> = V <sub>SS</sub> = -5V, R <sub>L</sub> = 1 kΩ, V <sub>IS</sub> = 5 V <sub>P-P</sub> , 20 Log <sub>10</sub> (V <sub>OS</sub> /V <sub>IS</sub> ) = -50 dB, (Figure 4)		1.25		MHz
	Crosstalk Between Any Two Switches (Frequency at -50 dB)	V <sub>DD</sub> = V <sub>C(A)</sub> = 5V; V <sub>SS</sub> = V <sub>C(B)</sub> = -5V, R <sub>L</sub> = 1 kΩ V <sub>IS(A)</sub> = 5 V <sub>P-P</sub> , 20 Log <sub>10</sub> (V <sub>OS(B)</sub> /V <sub>OS(A)</sub> ) = -50 dB, (Figure 5)		0.9		MHz
	Crosstalk; Control Input to Signal Output	V <sub>DD</sub> = 10V, R <sub>L</sub> = 10 kΩ R <sub>IN</sub> = 1 kΩ, V <sub>CC</sub> = 10V Square Wave, C <sub>L</sub> = 50 pF (Figure 6)		150		mV <sub>P-P</sub>
	Maximum Control Input	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 50 pF, (Figure 7) V <sub>OS(f)</sub> = ½ V <sub>OS</sub> (1 kHz) V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		6.5 8.0 9.0		MHz MHz MHz
C <sub>IS</sub>	Signal Input Capacitance			4		pF
C <sub>OS</sub>	Signal Output Capacitance	V <sub>DD</sub> = 10V		4		pF
C <sub>IOS</sub>	Feedthrough Capacitance	V <sub>C</sub> = 0V		0.2		pF
C <sub>IN</sub>	Control Input Capacitance			5	7.5	pF
<p><b>Note 4:</b> AC Parameters are guaranteed by DC correlated testing.</p> <p><b>Note 5:</b> These devices should not be connected to circuits with the power "ON".</p> <p><b>Note 6:</b> In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C<sub>L</sub> wherever it is specified.</p> <p><b>Note 7:</b> V<sub>IS</sub> is the voltage at the in/out pin and V<sub>OS</sub> is the voltage at the out/in pin. V<sub>C</sub> is the voltage at the control input.</p>						

AC Test Circuits and Switching Time Waveforms

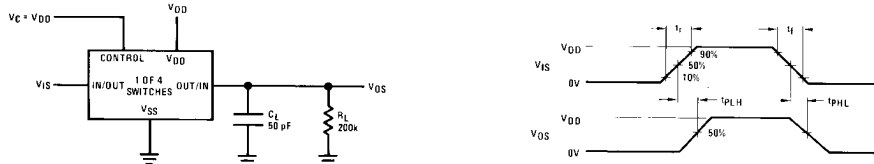


FIGURE 1.  $t_{PLH}$ ,  $t_{PLH}$  Propagation Delay Time Control to Signal Output

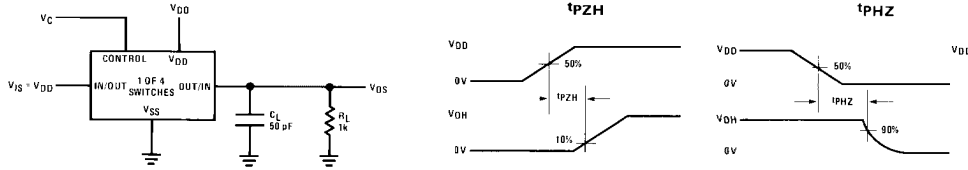


FIGURE 2.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output

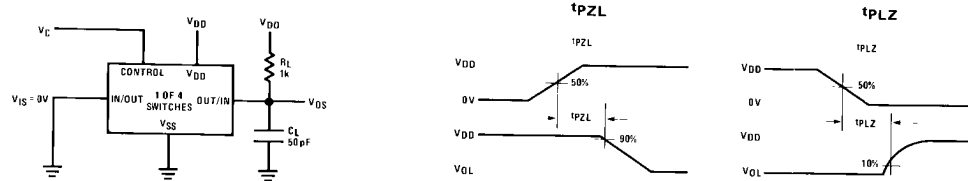
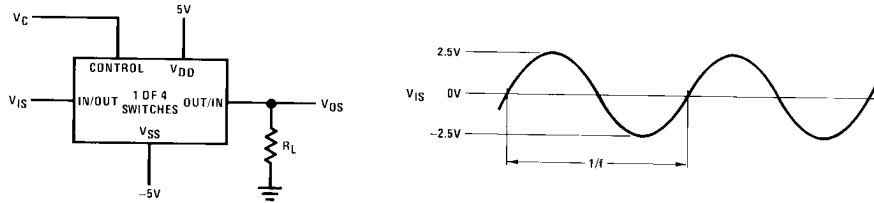


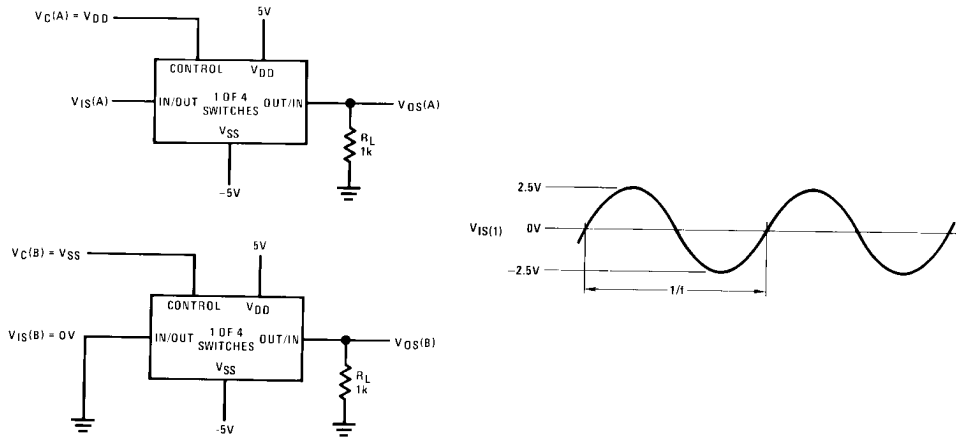
FIGURE 3.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output



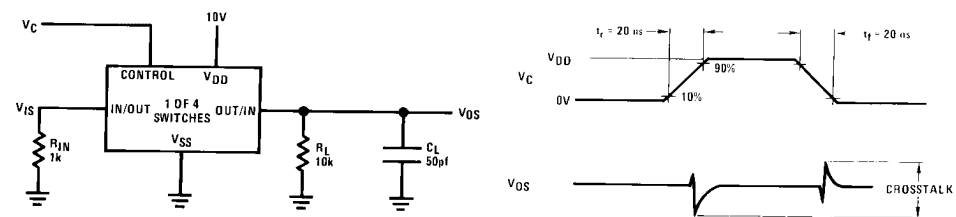
$V_C = V_{DD}$  for distortion and frequency response tests  
 $V_C = V_{SS}$  for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

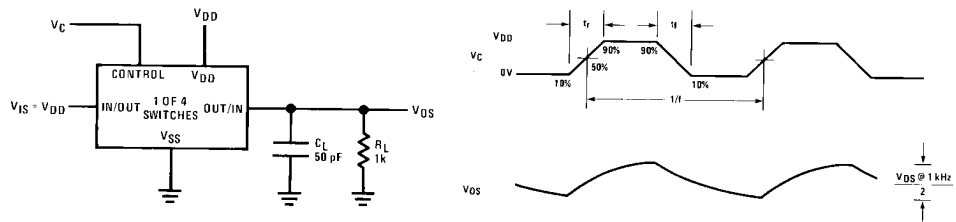
**AC Test Circuits and Switching Time Waveforms** (Continued)



**FIGURE 5. Crosstalk Between Any Two Switches**



**FIGURE 6. Crosstalk — Control to Input Signal Output**



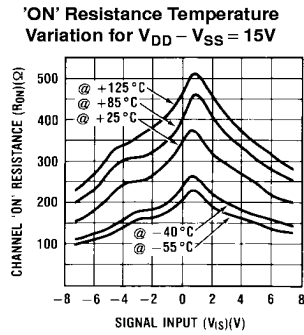
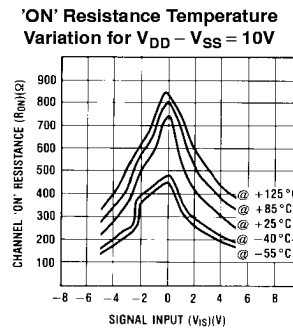
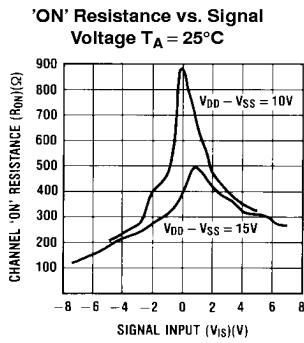
**FIGURE 7. Maximum Control Input Frequency**

AC Test Circuits and Switching Time Waveforms (Continued)

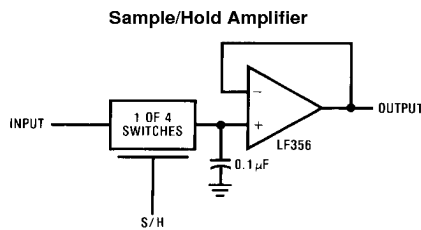
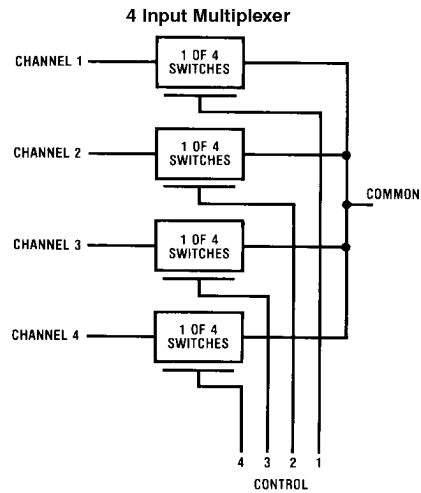
Temperature Range	V <sub>DD</sub>	Switch Input				Switch Output	
		V <sub>IS</sub>	I <sub>IS</sub> (mA)			V <sub>OS</sub> (V)	
			-40°C	25°C	+85°C	Min	Max
COMMERCIAL	5	0	0.2	0.16	0.12	4.6	0.4
	5	5	-0.2	-0.16	-0.12		
	10	0	0.5	0.4	0.3		0.5
	10	10	-0.5	-0.4	-0.3		
	15	0	1.4	1.2	1.0		1.5
	15	15	-1.4	-1.2	-1.0	13.5	

FIGURE 8. CD4016B Switch Test Conditions for V<sub>IHC</sub>

Typical Performance Characteristics



**Typical Applications**

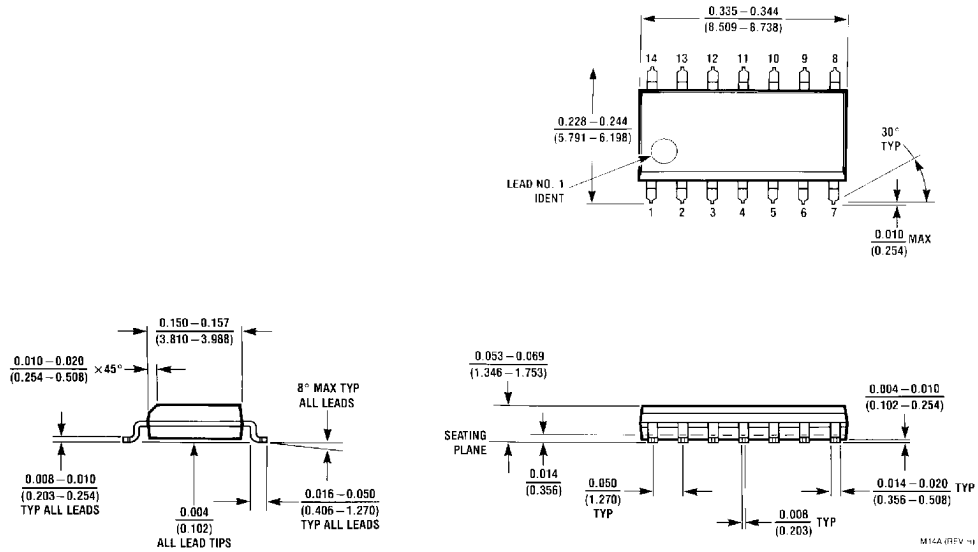


**Special Considerations**

The CD4016B is composed of 4, two-transistor analog switches. These switches do not have any linearization or compensation circuitry for "R<sub>ON</sub>" as do the CD4066B's. Because of this, the special operating considerations for the CD4066B do not apply to the CD4016B, but at low supply voltages, ≤5V, the CD4016B's on resistance becomes

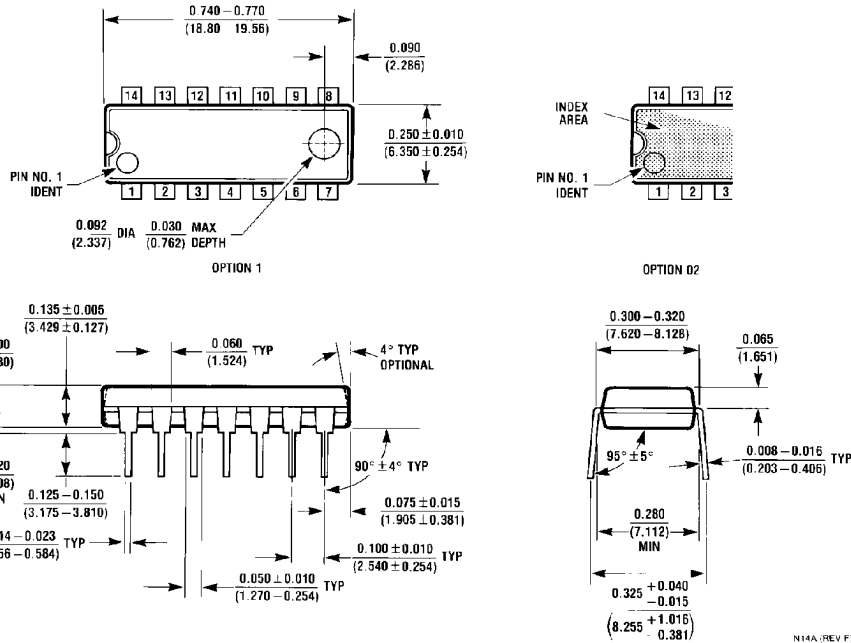
non-linear. It is recommended that at 5V, voltages on the in/out pins be maintained within about 1V of either V<sub>DD</sub> or V<sub>SS</sub>; and that at 3V the voltages on the in/out pins should be at V<sub>DD</sub> or V<sub>SS</sub> for reliable operation.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow  
Package Number M14A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N14A

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