

GD4727B

7-STAGE COUNTER

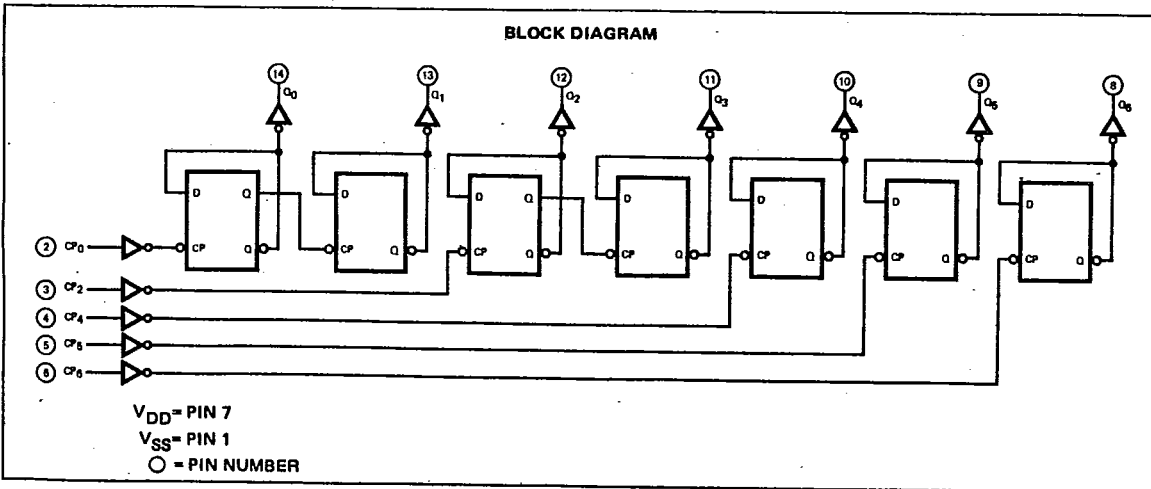
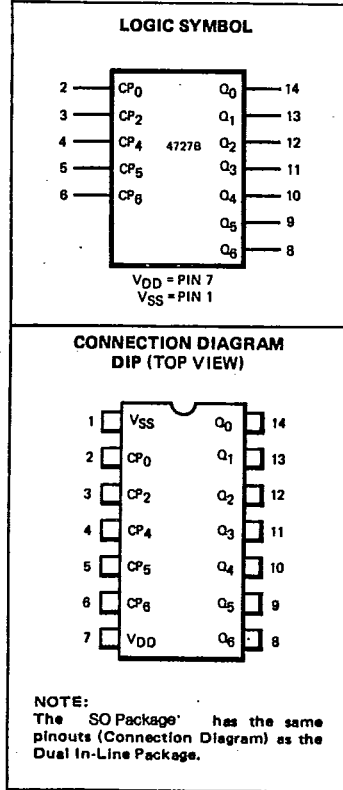
DESCRIPTION — The 4727B is a 7-Stage Frequency Counter especially useful for frequency synthesis in musical applications. The device is designed to generate, from a primary chromatic scale, each of the twelve flats, sharps, and naturals comprising each chromatic scale of the seven additional octaves in the musical spectrum. Twelve 4727B devices are required to generate the entire musical spectrum from a primary scale.

The 4727B consists of a pair of 2-Bit Counters, with Clock Inputs (CP₀ and CP₂) and Parallel Outputs (Q₀ and Q₁, Q₂ and Q₃), available, and three 1-bit counters, also with Clock Inputs (CP₄, CP₅, and CP₆) and Parallel Outputs (Q₄, Q₅, and Q₆) available. Each counter advances on a LOW-to-HIGH transition at the appropriate Clock Input.

- REPEATS A PRIMARY MUSICAL NOTE OR HALF NOTE IN SEVEN OCTAVES
- CLOCK INPUT EDGE — TRIGGERED ON THE LOW-TO-HIGH TRANSITION
- BUFFERED OUTPUTS AVAILABLE FROM ALL SEVEN STAGES

PIN NAMES

CP₀-CP₆ CLOCK INPUTS (L→H TRIGGERED)
 Q₀-Q₆ PARALLEL OUTPUTS



GS CMOS · GD4727B

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

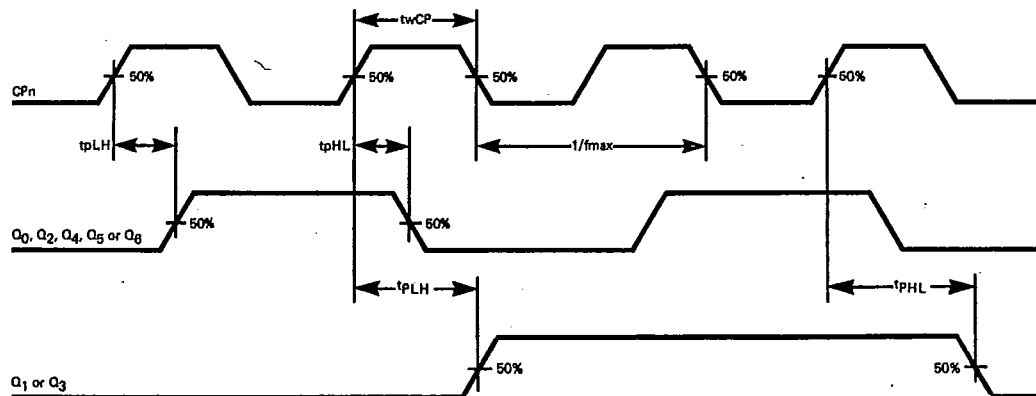
SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS	
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V						
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
I_{OH}	Output High Current	-0.3			-0.84			-1.8			mA	MIN 25°C MAX	$V_{OUT} = 4.5$ V For $V_{DD} = 5$ V. $V_{OUT} = 9.5$ V For $V_{DD} = 10$ V. $V_{OUT} = 13.5$ V For $V_{DD} = 15$ V.	Inputs at V_{SS} or V_{DD} Per the Logic Function or Truth Table
		-0.25			-0.7			-1.5						
		-0.2			-0.56			-1.1						
I_{OL}	Output Low Current	0.64			1.6			4.2			mA	MIN 25°C MAX	$V_{OUT} = 0.4$ V for $V_{DD} = 5$ V $V_{OUT} = 0.5$ V for $V_{DD} = 10$ V $V_{OUT} = 1.5$ V for $V_{CC} = 15$ V	
		0.51			1.3			3.4						
		0.36			0.9			2.4						
I_{DD}	Quiescent Power	XC			20			40			μ A	MIN, 25°C MAX	All Inputs at V_{DD} or V_{SS}	
					150			300						
	Supply Current	XM			5			10			μ A	MIN, 25°C MAX		
					150			300						

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_n to Q_0, Q_2, Q_4, Q_5 or Q_6		225	500		90	250		75	200	ns	$C_L = 50$ pF $R_L = 200$ k Ω Input Transition Times < 20 ns
t_{PHL}	CP _n to Q_1 or Q_3		225	500		90	250		75	200		
t_{PLH}	Propagation Delay, CP_n to Q_1 or Q_3		365	1000		130	500		100	400	ns	
t_{PHL}	CP _n to Q_1 or Q_3		365	1000		130	500		100	400		
t_{TLH}	Output Transition Times		70	500		40	250		30	200	ns	
t_{THL}	Output Transition Times		70	500		40	250		30	200		
T_{wCP}	Min Clock Pulse Width	250	125		125	65		100	50		ns	
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	8		5	10		MHz	

- NOTES:
- Additional DC characteristics are listed in this section under "4000B Series CMOS Family Characteristics."
 - Propagation Delays and Output Transition Times are graphically described in this section under "4000B Series CMOS Family Characteristics."
 - For f_{MAX} Input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.

SWITCHING WAVEFORMS



PROPAGATION DELAY, CP to Q_n, MINIMUM CLOCK PULSE WIDTH AND MAXIMUM FREQUENCY