GD4727B
7-STAGE COUNTER

DESCRIPTION – The 4727B is a 7-Stage Frequency Counter especially useful for frequency synthesis in musical applications. The device is designed to generate, from a primary chromatic scale, each of the twelve flats, sharps, and naturals comprising each chromatic scale of the seven additional octaves in the musical spectrum. Twelve 4727B devices are required to generate the entire musical spectrum from a primary scale.

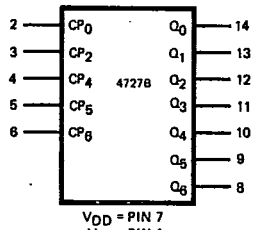
The 4727B consists of a pair of 2-Bit Counters, with Clock Inputs (CP_0 and CP_2) and Parallel Outputs (Q_0 and Q_1, Q_2 and Q_3), available, and three 1-bit counters, also with Clock Inputs (CP_4, CP_5, and CP_6) and Parallel Outputs (Q_4, Q_5, and Q_6) available. Each counter advances on a LOW-to-HIGH transition at the appropriate Clock Input.

- **REPEATS A PRIMARY MUSICAL NOTE OR HALF NOTE IN SEVEN OCTAVES**
- **CLOCK INPUT EDGE – TRIGGERED ON THE LOW-TO-HIGH TRANSITION**
- **BUFFERED OUTPUTS AVAILABLE FROM ALL SEVEN STAGES**

PIN NAMES

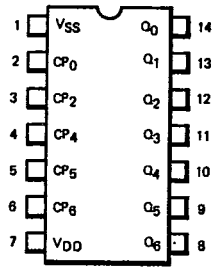
CP_0–CP_6	CLOCK INPUTS (L→H TRIGGERED)
Q_0–Q_6	PARALLEL OUTPUTS

LOGIC SYMBOL



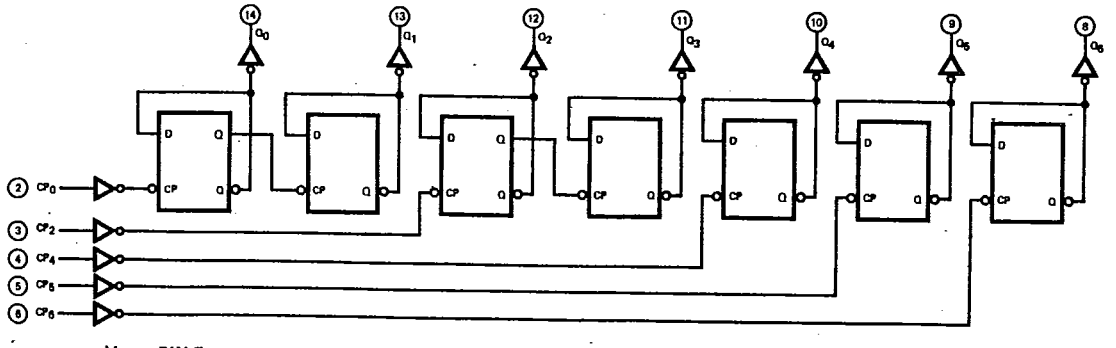
V_{DD} = PIN 7
V_{SS} = PIN 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-Line Package.

BLOCK DIAGRAM



V_{DD} = PIN 7
V_{SS} = PIN 1
○ = PIN NUMBER

GS CMOS · GD4727B

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

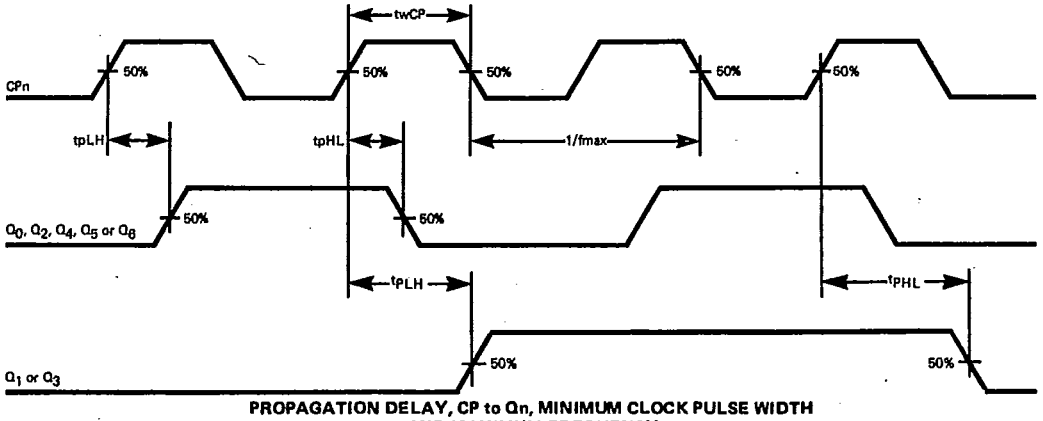
SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OH}	Output High Current		−0.3 −0.25 −0.2			−0.84 −0.7 −0.56			−1.8 −1.5 −1.1			mA	MIN 25°C MAX	V_{OUT} = 4.5 V For V_{DD} = 5 V. V_{OUT} = 9.5 V For V_{DD} = 10 V. V_{OUT} = 13.5 V For V_{DD} = 15 V. Inputs at V_{SS} or V_{DD} Per the Logic Function or Truth Table
I_{OL}	Output Low Current		0.64 0.51 0.36			1.6 1.3 0.9			4.2 3.4 2.4			mA	MIN 25°C MAX	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V V_{OUT} = 1.5 V for V_{CC} = 15 V
I_{DD}	Quiescent Power Supply Current	XC			20 150			40 300			80 600	μA	MIN,25°C MAX	All inputs at V_{DD} or V_{SS}
		XM			5 150			10 300			20 600	μA	MIN,25°C MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, CP_n to Q_0, Q_2, Q_4, Q_5 or Q_6		225 225	500 500		90 90	250 250		75 75	200 200	ns	C_L = 50 pF R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP_n to Q_1 or Q_3		365 365	1000 1000		130 130	500 500		100 100	400 400	ns	
t_{TLH} t_{THL}	Output Transition Times		70 70	500 500		40 40	250 250		30 30	200 200	ns	
T_{WCP}	Min Clock Pulse Width	250	125		125	65		100	50		ns	
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	8		5	10		MHz	

NOTES:
1. Additional DC characteristics are listed in this section under "4000B Series CMOS Family Characteristics."
2. Propagation Delays and Output Transition Times are graphically described in this section under "4000B Series CMOS Family Characteristics."
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.

SWITCHING WAVEFORMS



PROPAGATION DELAY, CP to Qn, MINIMUM CLOCK PULSE WIDTH AND MAXIMUM FREQUENCY