

64K (8K x 8) High Speed CMOS UV Erasable PROM

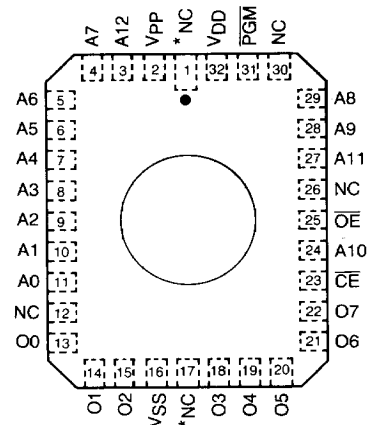
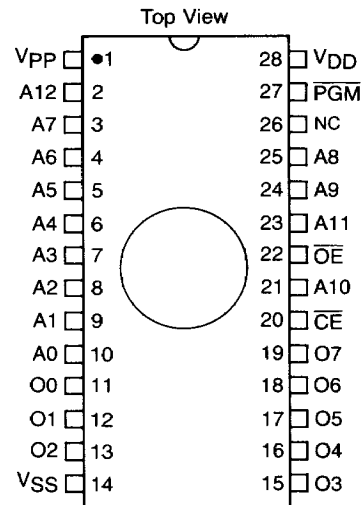
FEATURES

- Bipolar Performance — 45ns Maximum Access Time
- CMOS Design — Low Power Dissipation
 - 80mA Active Current
 - 100µA Standby Current (Low Power Option)
- OTP (One Time Programming) Available
- Auto-Insertion-Compatible Plastic Packages
- Auto ID™ Identification; Aids Automated Programming
- Separate Chip Enable and Output Enable Control Inputs
- Two Programming Algorithms Allow Improved Programming Times
 - Fast Programming
 - Rapid-Pulse Programming
- Organized 8K x 8 — JEDEC Standard Pinouts
 - 28 Pin Dual In Line Package
 - 32 Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
 - Commercial (C) = 0° to 70°C
 - Industrial (I) = -40° to 85°C
 - Military** (M) = -55° to +125°C

DESCRIPTION

The General Instrument Microelectronics 27HC64 is a CMOS 64K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). An advanced CMOS design allow bipolar speed with a significant reduction in power over bipolar PROMs. A low power option (L) allows further standby power reduction to 100µA. The 27HC64 is configured in a standard 64K EPROM pinout, which allows an easy upgrade for 27C64 sockets. This very high speed device allows digital signal processors (DSP) or other sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

PIN CONFIGURATION



- Pin 1 indicator on PLCC on top of package
- * DC (don't connect on PLCC package)

34

Res
006040

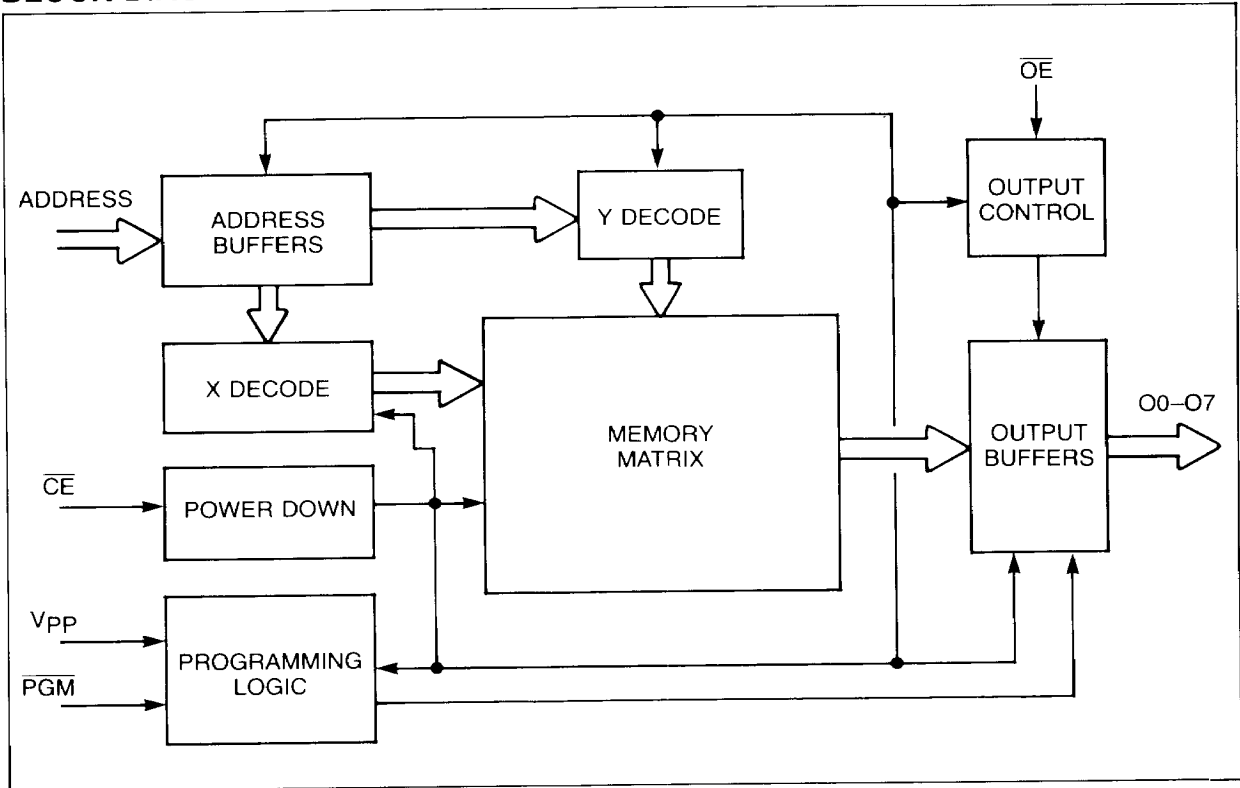
orig

6040

GI

**Military Version (MR) screened to MIL STD 883
Rev. C, Method 5004 Test Specification.

BLOCK DIAGRAM



MODES

MODES	CE	OE	PGM	Vpp	A9	O0-O7
Read	V _{IL}	V _{IL}	V _{IH}	V _{DD}	X	D _{out}
Program	V _{IL}	V _{IH}	V _{IL}	V _H	X	D _{in}
Program Verify	V _{IL}	V _{IL}	V _{IH}	V _H	X	D _{out}
Program Inhibit	V _{IH}	X	X	V _H	X	High Z
Standby	V _{IH}	X	X	V _{DD}	X	High Z
Output Disable	V _{IL}	V _{IH}	V _{IH}	V _{DD}	X	High Z
Identity	V _{IL}	V _{IL}	V _{IH}	V _{DD}	V _H	Identity Code

READ MODE (See Timing Diagrams and AC Characteristics)

Read mode is accessed when

- the \overline{CE} pin is low to power up (enable) the chip
- the \overline{OE} pin is low to gate the data to the output pins.

For Read operations on the low powered version, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). A faster \overline{CE} access time (t_{CE}) is available on the standard part to provide the additional time for decoding of the \overline{CE} signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of \overline{OE} .

STANDBY MODE

The standby mode is defined when the \overline{CE} pin is high and a program mode is not defined.

When these conditions are met, the supply current will drop from 80mA to 100 μ A on the low power part and to 40mA on the standard part.

OUTPUT ENABLE

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when

- The \overline{OE} pin is high and a program mode is not defined.

ERASE MODE

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1" 's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second / cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 μ W/cm² for 20 minutes.

PROGRAMMING MODE

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. The fast programming algorithm is recommended for windowed product only. A flowchart of the fast programming algorithm is shown in Figure 1.

The rapid-pulse programming algorithm has been developed to improve on the programming throughput times in a production environment. Up to 25 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the rapid-pulse programming algorithm is shown in Figure 2.

Rapid-pulse is the preferred programming algorithm.

Programming takes place when

- V_{PP} is brought to proper V_H level,
- V_{DD} is brought to proper voltage,
- the \overline{CE} pin is low,
- the \overline{PGM} pin is low, and
- the \overline{OE} pin is high.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0–A12 and the data to be programmed is presented to pins O0–O7. When data and address are stable, \overline{OE} is high, \overline{CE} is low and a low-going pulse on the \overline{PGM} line programs that location.

VERIFY

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- V_{PP} is at the proper V_H level,
- V_{DD} is at the proper level,
- the \overline{CE} line is low,
- the \overline{PGM} line is high, and
- the \overline{OE} line is low.

INHIBIT

When programming multiple devices in parallel with different data, only \overline{CE} need be under separate control to each device. By pulsing the \overline{CE} line low on a particular device in conjunction with the \overline{PGM} line low, that device will be programmed; all other devices with \overline{CE} held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on \overline{CE} or \overline{PGM}); and the device is inhibited from programming.

MANUFACTURERS IDENTITY

In this mode specific data is outputted that identifies the manufacturer as General Instrument Microelectronics, and device type. This mode is entered when Pin (A9) is taken up to between 11.5–12.5V. The \overline{CE} and \overline{OE} lines must be at V_{IL} . A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

The General Instrument Microelectronics identity code is as follows:

Identity \ Pin	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Code
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	0	0	1	91

*Code subject to change.

**ELECTRICAL CHARACTERISTICS
Maximum Ratings***

- V_{DD} and input voltages w.r.t. V_{SS} -0.6 to +6.25V
- V_{pp} voltage w.r.t. V_{SS} during programming -0.6 to +14V
- Voltage on A9 w.r.t. V_{SS} -0.6 to +13.5V
- Storage temperature. -65°C to +150°C
- Ambient temperature with power applied . -65°C to +125°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Set Up Conditions for DC Characteristics (Read Operation)

- $V_{DD} = +5V \pm 10\%$
- T_{AMB} : Commercial (C) = 0°C to 70°C
- Industrial (I) = -40°C to +85°C
- Military (M) = -55°C to +125°C

DC CHARACTERISTICS (READ OPERATION)

PARAMETER	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs Address lines A0–A12 Data lines (program mode) O0–O7 PGM \overline{CE} & \overline{OE} Logic "1" Logic "0" Leakage	V_{IH} V_{IL} I_{IL}	2.0 –0.1 –10	$V_{DD}+1$ 0.8 10	V V μA	$V_{IN} = 0$ to V_{DD}
Input Capacitance	C_{IN}		6	pF	$V_{IN} = 0V$, $T_{AMB} = 25^{\circ}C$, $f = 1MHz$
Outputs In read/verify mode O0–O7 Logic "1" Logic "0" Leakage	V_{OH} V_{OL} I_{OL}	2.4 –10	0.45 10	V V μA	$I_{OH} = -4.0mA$ $I_{OL} = 16.0mA$ $V_{OUT} = 0$ to V_{DD}
Output Capacitance	C_{OUT}		12	pF	$V_{OUT} = 0V$, $T_{AMB} = 25^{\circ}C$, $f = 1MHz$
Power Supply Current I_{DD} Active (TTL Inputs)	I_{DD}		80	mA	$V_{DD} = 5.5V$, $V_{PP} = V_{DD}$, $f = 2 MHz$, $\overline{OE} = \overline{CE} = V_{IL}$, $I_{OUT} = 0mA$, $T_{AMB} = 0^{\circ}C$ to $70^{\circ}C$, $V_{IL} = -0.1V$ to $0.8V$, $V_{IH} = 2.0V$ to V_{DD} ; (Note 2)
I_{DD} Active (TTL Inputs) (Extended Temp. Range)	I_{DD}		90	mA	$V_{DD} = 5.5V$, $V_{PP} = V_{DD}$, $f = 2 MHz$, $\overline{OE} = \overline{CE} = V_{IL}$, $I_{OUT} = 0mA$, $T_{AMB} = -55^{\circ}C$ to $125^{\circ}C$, $V_{IL} = -0.1V$ to $0.8V$, $V_{IH} = 2.0V$ to V_{DD} ; (Note 3)
I_{DD} Standby (TTL Inputs) Standard Power Part	$I_{DD(S)TTL}$		40	mA	$\overline{CE} = V_{IH}$ $T_{AMB} = 0^{\circ}C$ to $70^{\circ}C$
I_{DD} Standby (TTL Inputs) (Extended Temperature Range) Standard Power Part	$I_{DD(S)TTL}$		50	mA	$\overline{CE} = V_{IH}$ $T_{AMB} = -55^{\circ}C$ to $125^{\circ}C$
I_{DD} Standby (TTL Inputs) Low Power Part	$I_{DD(SL)TTL}$		2	mA	$\overline{CE} = V_{IH}$ $T_{AMB} = 0^{\circ}C$ to $70^{\circ}C$
I_{DD} Standby (TTL Inputs) (Extended Temperature Range) Low Power Part	$I_{DD(SL)TTL}$		3	mA	$\overline{CE} = V_{IH}$ $T_{AMB} = -55^{\circ}C$ to $125^{\circ}C$
I_{DD} Standby (CMOS Inputs) Low Power Part	$I_{DD(SL)CMOS}$		100	μA	$\overline{CE} = V_{DD} \pm 0.2V$
I_{PP} (Read Mode) V_{PP} READ VOLTAGE	V_{PP}	$V_{DD}-0.7$	V_{DD}	μA V	$V_{PP} = 5.5V$ (NOTE 1)

Note: (1) V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 (2) A.C. power component for frequency above 2 MHz is 3mA/MHz.
 (3) A.C. power component for frequency above 2 MHz is 5mA/MHz (Extended Temp Range).

AC CHARACTERISTICS (Read Operation)

T_A: Commercial (C) = 0°C to 70°C
 Industrial (I) = -40°C to +85°C
 Military (M) = -55°C to +125°C

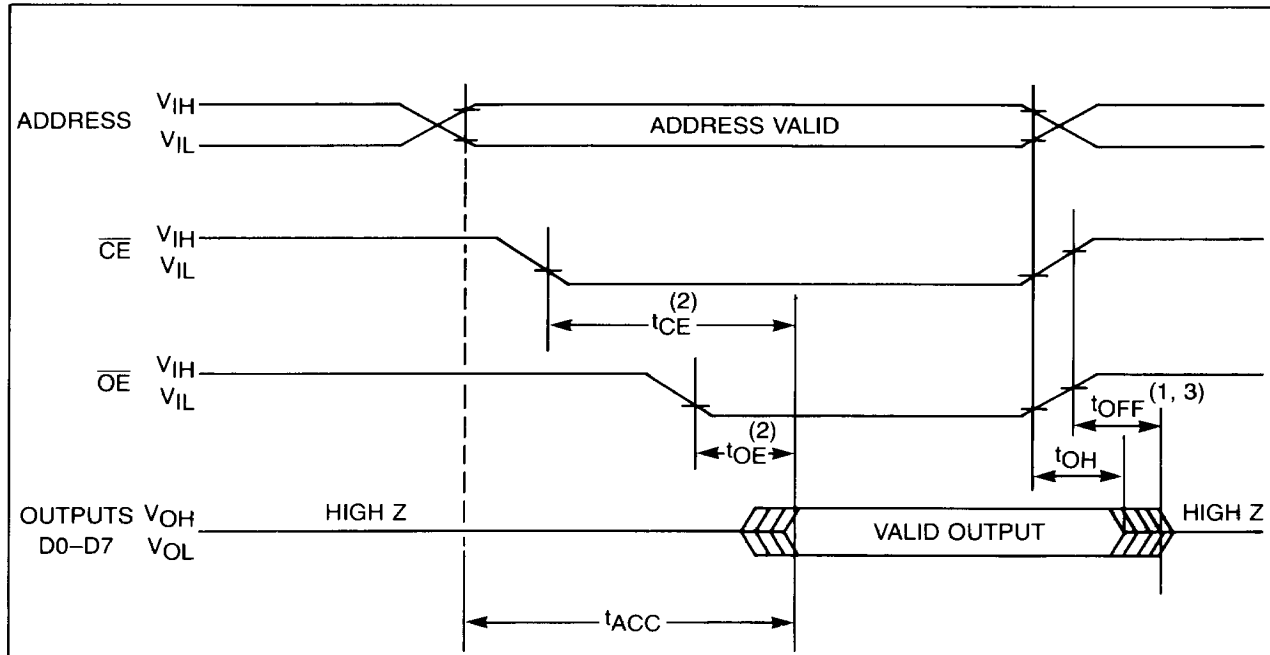
AC TESTING WAVEFORM
 V_{IH} = 2.4V AND V_{IL} = 0.45V
 V_{OH} = 2.0V AND V_{OL} = 0.8V
 Output Load = 1 TTL Load + 100pF

Note: 27HC64-45 is only available in commercial temperature range.

SYM	PARAMETER	27HC64-45		27HC64-55		27HC64-70		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t _{ACC}	Address to Output Delay		45		55		70	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t _{CE1} ¹	\overline{CE} to Output Delay		30		35		45	ns	$\overline{OE} = V_{IL}$
t _{CE2} ¹	\overline{CE} to Output Delay		45		55		70	ns	$\overline{OE} = V_{IL}$
t _{OE}	\overline{OE} to Output Delay		20		20		25	ns	$\overline{CE} = V_{IL}$
t _{OFF}	\overline{OE} to O/P High Impedance	0	20	0	20	0	25	ns	$\overline{CE} = V_{IL}$
t _{OH}	Output Hold From Address \overline{CE} or \overline{OE} , whichever goes first	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: (1) t_{CE1} is for standard power and t_{CE2} is for low power part

READ WAVEFORMS



- Notes: (1) t_{OFF} is specified for \overline{OE} or \overline{CE} , whichever occurs first.
 (2) \overline{OE} may be delayed up to t_{CE} - t_{OE} after the falling edge of \overline{CE} without impact on t_{CE}.
 (3) This parameter is sampled and is not 100% tested.

DC PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5^\circ\text{C}$ (see programming algorithm for V_{DD} & V_{PP} voltages)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS (SEE NOTE 1)
I_{LI}	Input Current (All Inputs)	-10	10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{DD} + 1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 16.0\text{mA}$
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -4.0\text{mA}$
I_{DD2}	V_{DD} Supply Current (Program & Verify)		80	mA	
I_{PP2}	V_{PP} Supply Current (Program)		40	mA	$\overline{CE} = V_{IL}$
V_{ID}	A9 Product Identification Voltage	11.5	12.5	V	

Note: (1) V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

AC PROGRAMMING CHARACTERISTICS

Conditions: 25°C ± 5°C (see programming algorithm for V_{DD} & V_{PP} voltages)

AC TESTING WAVEFORM

V_{IH} = 2.4V and V_{IL} = 0.45V

V_{OH} = 2.0V and V_{OL} = 0.8V

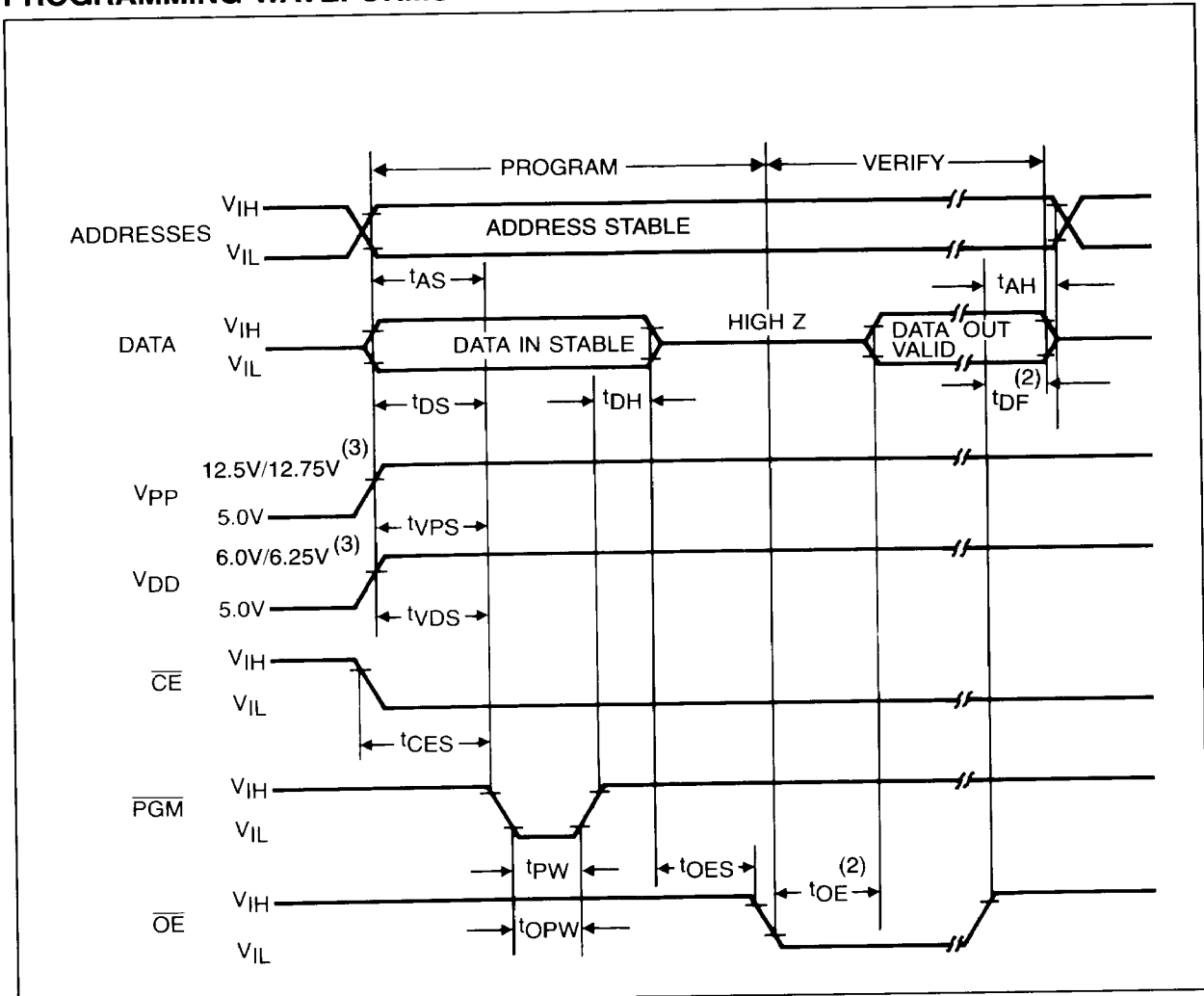
Output Load = 1 TTL Load + 100pF

Program, Program Verify, and Program Inhibit Modes

PARAMETER	SYM	MIN	TYP	MAX	UNITS
Address Setup-Up Time	t _{AS}	2			μs
Data Set-Up Time	t _{DS}	2			μs
Data Hold Time	t _{DH}	2			μs
Address Hold Time	t _{AH}	0			μs
Float Delay ³	t _{DF}	0		130	ns
V _{DD} Set-Up Time	t _{VDS}	2			μs
Program Pulse Width ¹	t _{PW}	0.95	1	1.05	ms
Program Pulse Width ¹	t _{PW}	95	100	105	μs
\overline{CE} Set-Up Time	t _{CES}	2			μs
\overline{OE} Set-Up Time	t _{OES}	2			μs
V _{PP} Set-Up Time	t _{VPS}	2			μs
Overprogram Pulse Width ²	t _{OPW}	2.85		78.75	ms
Data valid from \overline{OE}	t _{OE}			100	ns

- Notes: (1) For rapid-pulse programming algorithm, initial programming width tolerance is 100 μsec ± 5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
- (2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
- (3) This parameter is only sampled and not 100% tested. Output float is defined at the point where data is no longer driven (see timing diagram).

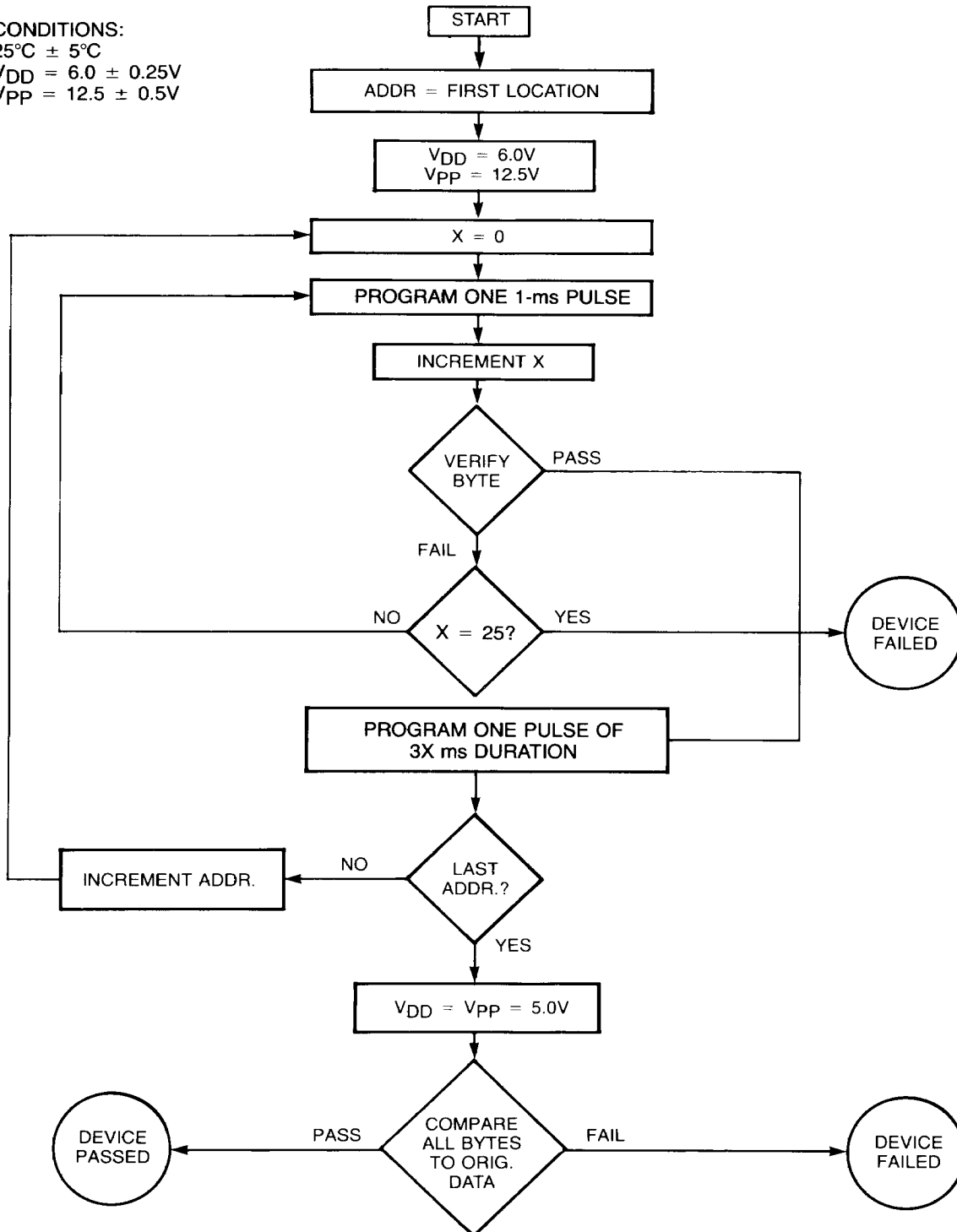
PROGRAMMING WAVEFORMS(1)



- Notes: (1) The input timing reference level is 0.8V for V_{IL} and 2V for V_{IH} .
 (2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
 (3) $V_{DD} = 6.0 \pm 0.25$, $V_{PP} = 12.5 \pm 0.5$ V for fast programming algorithm
 $V_{DD} = 6.25 \pm 0.25$, $V_{PP} = 12.75 \pm 0.25$ V for rapid-pulse programming algorithm.

FAST PROGRAMMING ALGORITHM (Figure 1)

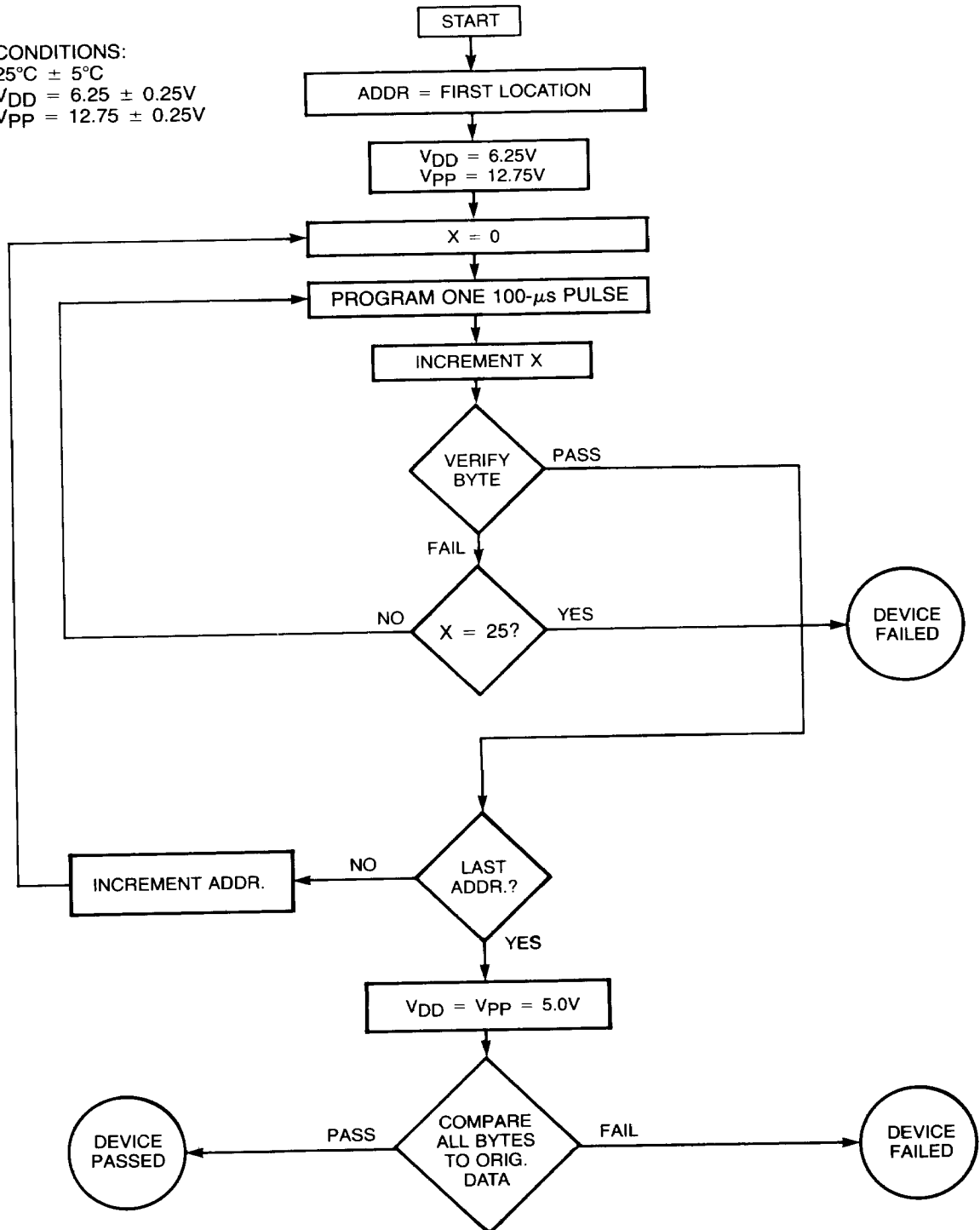
CONDITIONS:
 $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$
 $V_{DD} = 6.0 \pm 0.25\text{V}$
 $V_{PP} = 12.5 \pm 0.5\text{V}$



RECOMMENDED FOR WINDOWED PRODUCT ONLY

RAPID-PULSE PROGRAMMING ALGORITHM (Figure 2)

CONDITIONS:
 $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$
 $V_{DD} = 6.25 \pm 0.25\text{V}$
 $V_{PP} = 12.75 \pm 0.25\text{V}$



ORDER INFORMATION

27HC64 - 45 M R / KA

PACKAGE

- CERDIP
- D SIDEBRAZED CERAMIC
- KA CERAMIC LEADLESS CHIP CARRIER
- KB CERAMIC LEADLESS CHIP CARRIER, THERMALLY ENHANCED
- L PLASTIC LEADED CHIP CARRIER
- P PLASTIC DIP

SCREENING

- STANDARD COMMERCIAL SCREENING
- R SCREENING PER MIL STD 883C METHOD 5004

TEMPERATURE RANGE

- 0°C TO 70°C
- I -40°C TO 85°C
- M -55°C TO 125°C

SPEED

- 45 45NS ACCESS
- 55 55NS ACCESS
- 70 70NS ACCESS

DEVICE

- 27HC64 64K (8K X 8) HIGH SPEED CMOS EPROM
- 27HC64L 64K (8K X 8) HIGH SPEED LOW POWER CMOS EPROM

GIM/Worldwide Sales Offices

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