

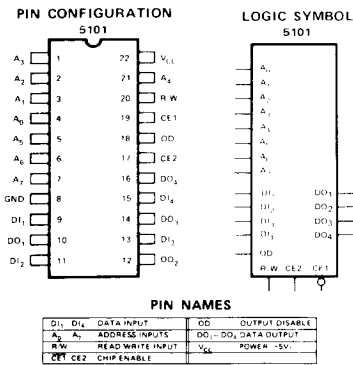
# M5101-4, M5101L-4

## 256 x 4 BIT STATIC CMOS RAM

- Military Temperature Range: -55°C to +125°C
- Ultra Low Standby Current: 200nA/Bit
- Fast Access Time — 800ns
- Single +5V Power Supply
- CE2 Controls Unconditional Standby Mode
- Three-State Output

The Intel® M5101 is an ultra-low power 256 X 4 CMOS RAM specified over the -55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. When deselected with CE2 low, the M5101 draws from the single 5-volt supply only 200 microamps at 125°C.

The Intel® M5101 is fabricated with an ion-implanted, silicon gate, Complementary MOS (CMOS) process. This technology allows the design and production of ultra-low power, high performance memories.



### ABSOLUTE MAXIMUM RATINGS\*

- Ambient Temperature Under Bias . . . . . -65°C to 135°C
- Storage Temperature . . . . . -65°C to +150°C
- Voltage On Any Pin . . . . .
- With Respect to Ground . . . . . -0.3V to V<sub>CC</sub> +0.3V
- Maximum Power Supply Voltage . . . . . +7.0V
- Power Dissipation . . . . . 1 Watt

*\*COMMENT:*

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D.C. AND OPERATING CHARACTERISTICS FOR M5101-4, M5101L-4

T<sub>A</sub> = -55°C to 125°C, V<sub>CC</sub> = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ. <sup>[1]</sup>	Max.	Unit	Test Conditions
I <sub>LI</sub> [2]	Input Current		8		nA	V <sub>IN</sub> = 0 to 5.25V
I <sub>LOH</sub> [2]	Output High Leakage			2	μA	CE1 = 2.2V, V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>LOL</sub> [2]	Output Low Leakage			2	μA	CE1 = 2.2V, V <sub>OUT</sub> = 0.0V
I <sub>CC1</sub>	Operating Current		11	25	mA	V <sub>IN</sub> = V <sub>CC</sub> Except CE1 ≤ 0.01V Outputs Open
I <sub>CC2</sub>	Operating Current		20	32	mA	V <sub>IN</sub> = 2.2V Except CE1 ≤ 0.5V Outputs Open
I <sub>CCL</sub> [2]	Standby Current		2	200	μA	V <sub>IN</sub> = 0 to V <sub>CC</sub> . Except CE2 ≤ 0.2V
V <sub>IL</sub>	Input "Low" Voltage	-0.3		0.5	V	
V <sub>IH</sub>	Input "High" Voltage	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V	
V <sub>OL</sub>	Output "Low" Voltage			0.4	V	I <sub>OL</sub> = 2.0mA
V <sub>OH</sub>	Output "High" Voltage	V <sub>CC</sub> -2.0			V	I <sub>OH</sub> = 1.0mA

NOTES: 1. Typical values are T<sub>A</sub> = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I<sub>CCL</sub>.

MILITARY TEMP.

Low V<sub>CC</sub> Data Retention Characteristics (For M5101L-4) T<sub>A</sub> = -55°C to 125°C

Symbol	Parameter	Min.	Typ. <sup>[1]</sup>	Max.	Unit	Test Conditions
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	2.0			V	CE2 ≤ 0.2V V <sub>DR</sub> = 2.0V
I <sub>CCDR</sub>	Data Retention Current		2	200	μA	
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	0			ns	
t <sub>R</sub>	Operation Recovery Time	t <sub>RC</sub> <sup>[2]</sup>			ns	

NOTES: 1. Typical values are T<sub>A</sub> = 25°C and nominal supply voltage.  
2. t<sub>RC</sub> = Read Cycle Time.

A.C. CHARACTERISTICS FOR M5101-4, M5101L-4

READ CYCLE T<sub>A</sub> = -55°C to 125°C, V<sub>CC</sub> = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t <sub>RC</sub>	Read Cycle	800			ns	(See below)
t <sub>A</sub>	Access Time			800	ns	
t <sub>CO1</sub>	Chip Enable (CE1) to Output			700	ns	
t <sub>CO2</sub>	Chip Enable (CE2) to Output			850	ns	
t <sub>OD</sub>	Output Disable To Output			350	ns	
t <sub>DF</sub>	Data Output to High Z State	0		150	ns	
t <sub>OH1</sub>	Previous Read Data Valid with Respect to Address Change	0			ns	
t <sub>OH2</sub>	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t <sub>WC</sub>	Write Cycle	800			ns	(See below)
t <sub>AW</sub>	Write Delay	150			ns	
t <sub>CW1</sub>	Chip Enable (CE1) To Write	550			ns	
t <sub>CW2</sub>	Chip Enable (CE2) To Write	550			ns	
t <sub>DW</sub>	Data Setup	400			ns	
t <sub>DH</sub>	Data Hold	100			ns	
t <sub>WP</sub>	Write Pulse	400			ns	
t <sub>WR</sub>	Write Recovery	50			ns	
t <sub>DS</sub>	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: 0.5 Volt to V<sub>CC</sub>-2.0 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

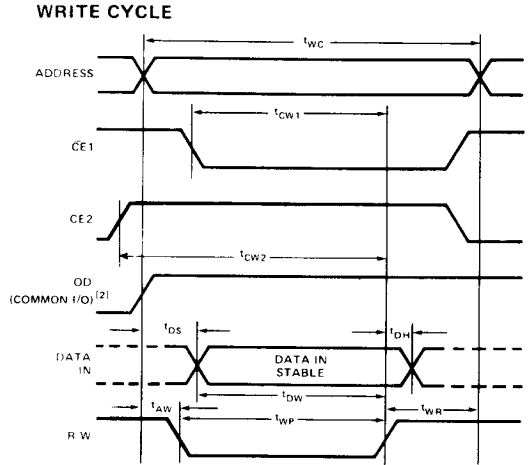
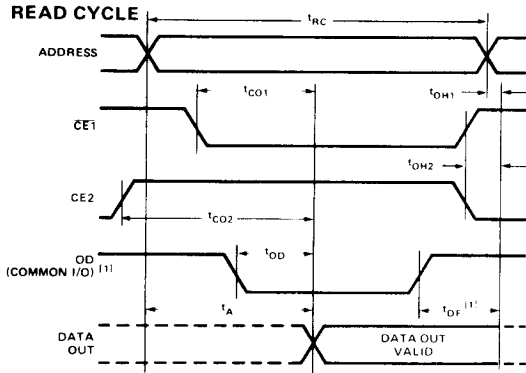
Output Load: 1 TTL Gate and C<sub>L</sub> = 100pF

CAPACITANCE<sup>[3]</sup> T<sub>A</sub> = 25°C, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C <sub>IN</sub>	Input Capacitance (All Input Pins) V <sub>IN</sub> = 0V	4	8
C <sub>OUT</sub>	Output Capacitance V <sub>OUT</sub> = 0V	8	12

NOTE: 3. This parameter is periodically sampled and is not 100% tested.

WAVEFORMS



- NOTES: 1. OD may be tied low for separate I/O operation.  
 2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low  $V_{CC}$  Data Retention

