1024-BIT (256-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

This is a 256-word by 4-bit static RAM fabricated with the silicon-gate CMOS process and designed for low power dissipation and easy application of battery back-up.

The device has two chip-select inputs $\overline{CS_1}$ and CS_2. While maintained in the chip non-select state, the device consumes power at the low value of only 1μA (max) standby current and accordingly is especially suitable as a memory system for battery-operated applications and for battery back-up.

The device operates on a single 5V supply, as does TTL, and inputs and outputs are directly TTL-compatible and are provided with common I/O terminals.

FEATURES

- Access time: 450ns (max)
- Low power dissipation in the standby mode: 5nW/bit (max)
- Single 5V power supply
- Data holding at 2V supply voltage
- No external clock or refreshing operation required
- Both inputs and outputs are directly TTL-compatible
- Outputs are three-state, with OR-tie capability
- Simple memory expansion by chip-select signals
- Input and output data terminals are separate
- Interchangeable with Intel's 5101L-1 in pin configuration and electrical characteristics

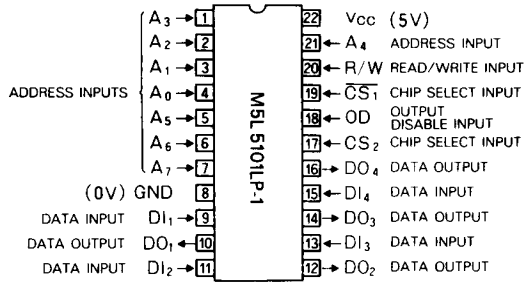
APPLICATION

- Battery-driven or battery back-up small-capacity memory units

FUNCTION

The device provides separate data input and output terminals.

PIN CONFIGURATION (TOP VIEW)



Outline 22P1

During a write cycle, when a location is designated by address signals A_0~A_7 and signal R/W goes low, the data of the DI inputs at that time is written.

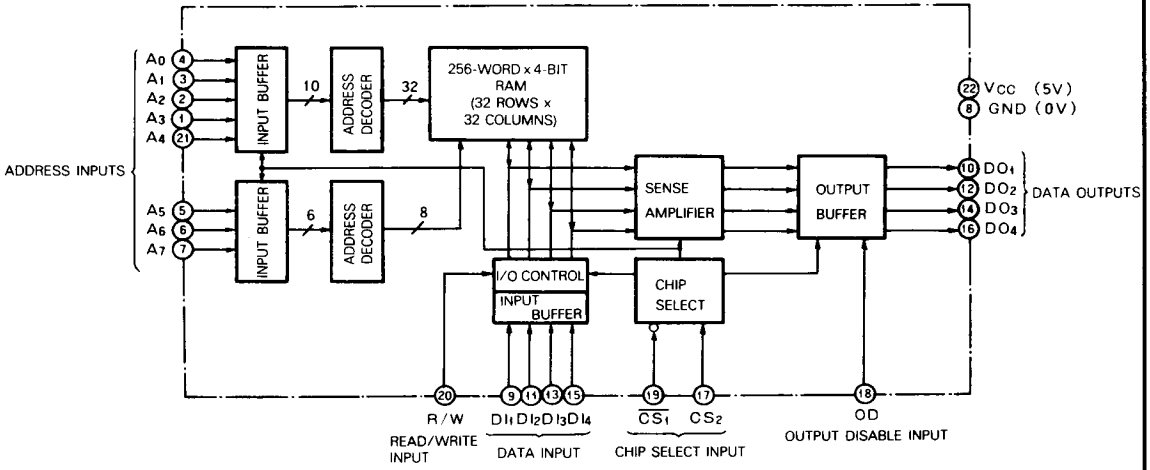
During a read cycle, when a location is designated by address signals A_0~A_7, and signal R/W goes high, the data of the designated address is available at the DO terminals.

When signal $\overline{CS_1}$ is high or CS_2 is low, the chip is in the non-selectable state, disabling both reading and writing. In this case, the output is in the floating (high-impedance state) useful for OR-ties with the output terminals of other chips.

When the signal OD is high, the output is in the floating state, so that OD is used as an input/output select control signal for common input/output operation.

The memory data can be held at a supply voltage of 2V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage	With respect to GND	−0.3 ~ V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0 ~ V_{CC}	V
P_d	Maximum power dissipation	T_a = 25°C	700	mW
Topr	Operating free-air ambient temperature range		0 ~ 70	°C
Tstg	Storage temperature range		−40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Low-level input voltage	−0.3		0.65	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{IL}	Low-level input voltage		−0.3		0.65	V
V_{OH}	High-level output voltage	I_{OH} = −1mA			0.4	V
V_{OL}	Low-level output voltage	I_{OL} = 2mA	2.4			V
I_I	Input current	V_I = 0 ~ 5.5V			±1	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS1})}$ = 2.2V, V_O = 2.4V ~ V_{CC}			1	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS1})}$ = 2.2V, V_O = 0.4V			−1	μA
I_{CC1}	Supply current from V_{CC}	$\overline{CS}_1 \leqq 0.01$V, other inputs = V_{CC}, Output open		9	22	mA
I_{CC2}	Supply current from V_{CC}	$\overline{CS}_1 \leqq 0.01$V, other inputs = 2.2V, Output open		13	27	mA
I_{CC3}	Supply current from V_{CC}	$CS_2 \leqq 0.2$V			1	μA
C_I	Input capacitance, all inputs	V_I = GND, V_I = 25mVrms, f = 1MHz		4	8	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz		8	12	pF

Note 1 : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Alt. symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(WR)}$	Write cycle time	t_{WC}	Input pulse V_{IH} = 2.2V V_{IL} = 0.65V tr = tf = 20ns Reference level = 1.5V Load = 1TTL, C_L = 100pF	450			ns
$t_{W(WR)}$	Write pulse width	t_{WP}		250			ns
$t_{su(AD)}$	Address setup time with respect to write pulse	t_{AW}		130			ns
t_{wr}	Write recovery time	t_{WR}		50			ns
$t_{su(OD)}$	OD setup time with respect to data-in	t_{DS}		130			ns
$t_{su(DA)}$	Data setup time	t_{DW}		250			ns
$t_{h(DA)}$	Data hold time	t_{DH}		50			ns
$t_{su(\overline{CS1})}$	Chip select setup time	t_{CW1}		350			ns
$t_{su(CS2)}$	Chip select setup time	t_{CW2}		350			ns

SWITCHING CHARACTERISTICS (For Read Cycle) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless without noted)

Symbol	Parameter	Alt. symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	t_{RC}	Input pulse V_{IH} = 2.2V V_{IL} = 0.65V tr = tf = 20ns Reference level = 1.5V Load = 1TTL, C_L = 100pF	450			ns
$t_{a(AD)}$	Address access time	t_A				450	ns
$t_{a(\overline{CS1})}$	Chip select access time	t_{CO1}				400	ns
$t_{a(CS2)}$	Chip select access time	t_{CO2}				500	ns
$t_{a(OD)}$	OD access time	t_{OD}				250	ns
t_{PXZ}	Output disable time (note 2)	t_{DF}				130	ns
$t_{dv(AD)}$	Data valid time with respect to address	t_{OH1}		0			ns

Note 2 : t_{PXZ} is from $\overline{CS}_1$, CS_2, or OD, whichever occurs first.

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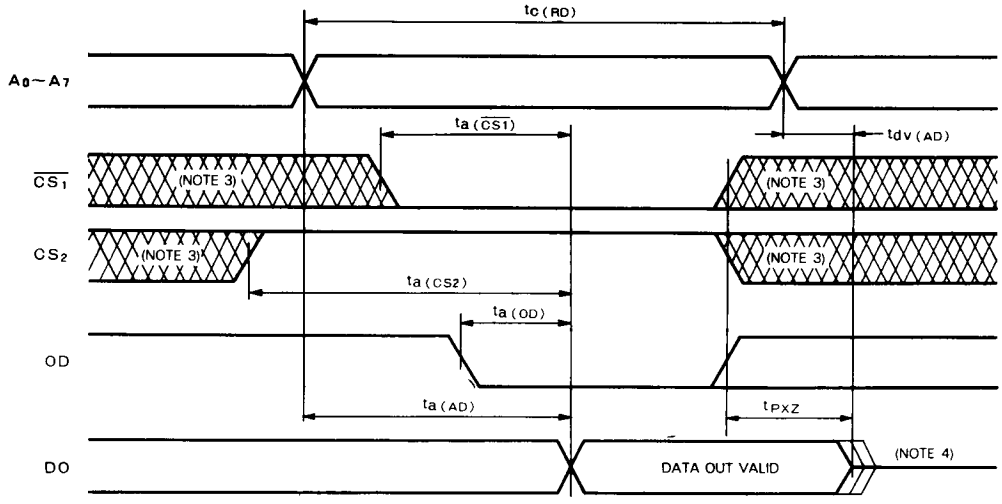
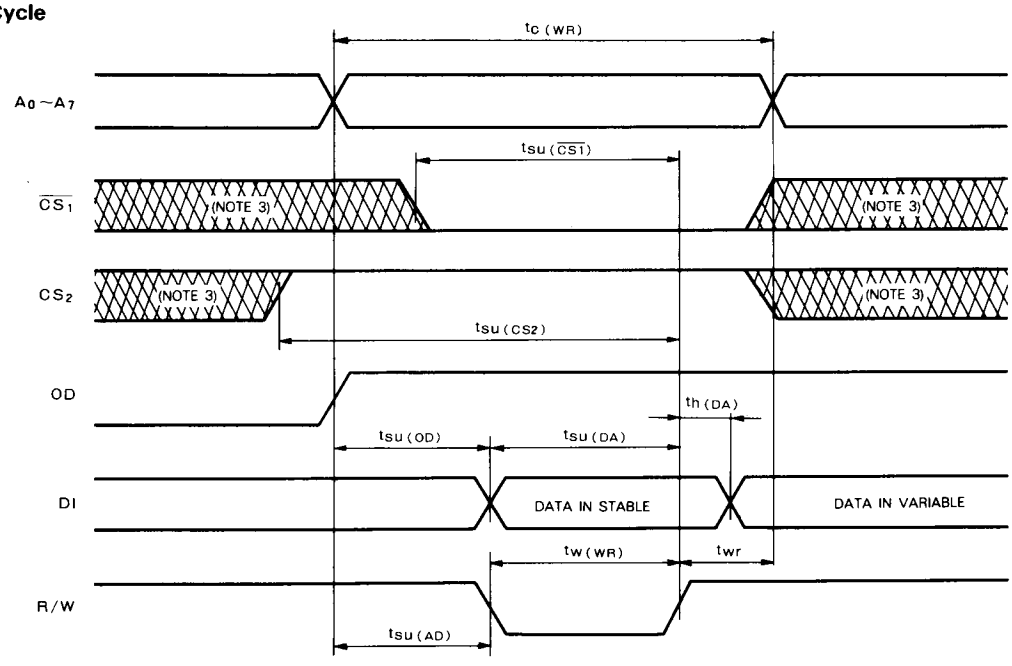
TIMING DIAGRAMS

Read Cycle

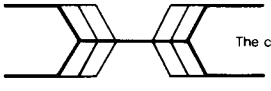


Write Cycle



Note 3 : Hatching indicates the state is unknown.

4 : Indicates that during this period the data-out is invalid for this definition of $t_{dv(AD)}$ and is in the floating state for this definition of t_{PXZ}.



The center line indicates a floating (high-impedance) state.

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POWER-DOWN OPERATION

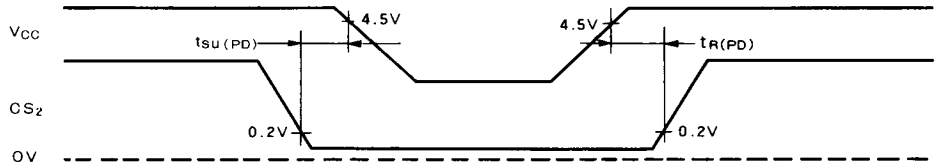
Electrical Characteristics ($T_a = 0 \sim 70°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		2			V
$V_I(\overline{CS})$	Power-down chip select input voltage	$2.2V \leqq V_{CC(PD)} \leqq V_{CC}$	2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$	$V_{CC(PD)}$			V
$I_{CC(PD)}$	Power-down supply current from V_{CC}	$V_{CC}=2V$, all inputs $=2V$			1	μA

Timing Requirements ($T_a = 0 \sim 70°C$, $V_{CC}=5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time	0			ns
$t_{R(PD)}$	Power-down recovery time	$t_{C(RD)}$			ns

Timing Diagram



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