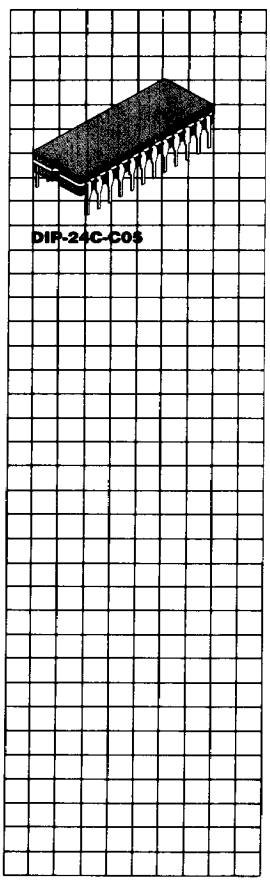
MB70802-20
4,608-Bit Buffer Address Array

Description

The Fujitsu MB70802 is a 4608-bit ECL read/write buffer address array which can be used for wider tag addresses or deeper tag memories. The device is organized as a high speed 512 words by 9-bits static RAM array, parity generator/checker, and 9-bit high speed comparator. It also features on-chip voltage compensation for improved noise margin.

The MB70802 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time, high yields, and outstanding device reliability are achieved in volume production.

Operation for the MB70802 is specified over a temperature range of from 0° to 75°C (ambient). It also features standard ceramic 24-pin dual-in-line packaging, and it is fully compatible with industry-standard 10K-series ECL families.

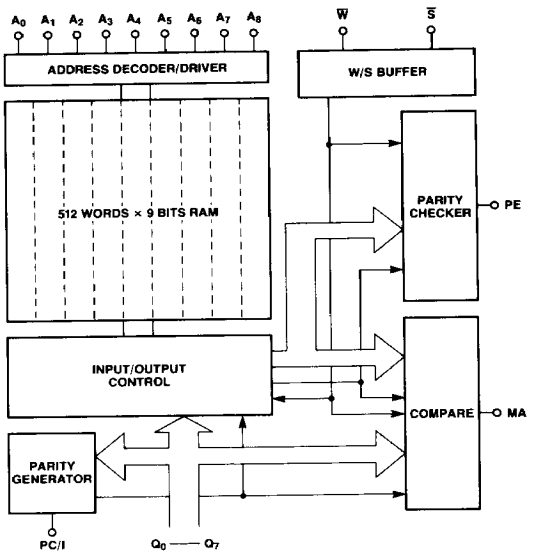


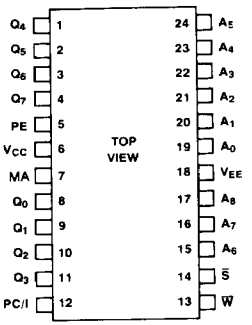
Features

- **512 words x 9-bits organization**
- **On-chip parity generator/checker**
- **9-bit high speed comparator.**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Parity Error address access time:**
  20 ns max.
  18 ns typ.
- **Match address access time:**
  20 ns max.
  18 ns typ.
- **Match data in access time:**
  15 ns max.
  12 ns typ.
- **Chip select access time:**
  10 ns max.
  6 ns typ.
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.25 mW/bit typ.**
- **DOPOS and IOP-II processing**

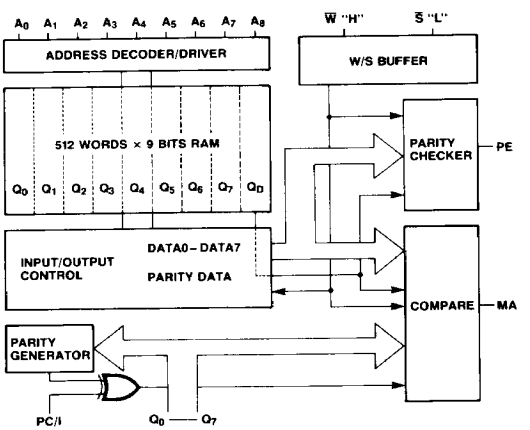
Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MB70802 Block Diagrams and Pin Assignment



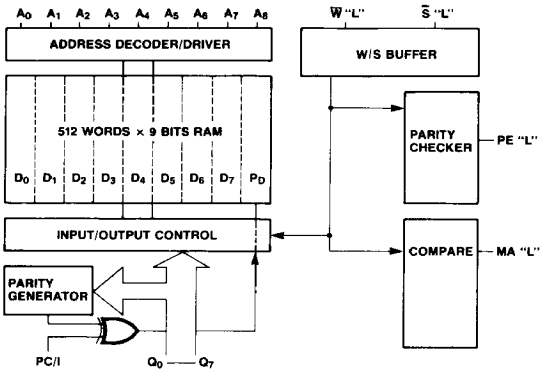


Read Operating Data—Signal Flow



MB70802 Block Diagram and Pin Assignment
(Continued)

Write Operating Data—Signal Flow



TRUTH TABLE

INPUT				OUTPUT		
PC/I	$\overline{S}$	$\overline{W}$	D_I	MATCH	PE	
X	H	X	X	L	L	DISABLE
PI	L	L	D_I	L	L	WRITE "D_I"
PI	L	H	D_I	L	PI	EQUAL (READ)
PI	L	H	D_I	L	$\overline{PI}$	UNDEFINED ERROR (READ)
PI	L	H	D_I	H	PI	NOT EQUAL (READ)
PI	L	H	D_I	H	$\overline{PI}$	PARITY ERROR (READ)

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
D_I = DATA IN
$\overline{PI}$ = H OR L
X = DON'T CARE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A	−55 to +125	°C
Storage temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Functional Description

The Fujitsu MB70802 is a 4,608-bit buffer address array organized as a high speed 512 words by 9-bits static RAM array, parity generator/checker, and 9-bit high speed comparator. Word selection is achieved by means of a 9-bit address designated A_0–A_8.

The active low chip select ($\overline{S}$) input is provided for memory array expansion. The read (Compare/Parity Checker) and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the 8-bit data on Q_0 to Q_7 and a parity bit data generated by parity generator are written into the addressed location. If a PC/I input holds low (high) under the write operation, a parity error flag is high (low) under the read operation. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. The 8-bit data and parity bit data are input to all the comparators which perform a match of the nine inputs (one word) against the stored word. If a particular word is identical to the input word, such comparators generate a match signal. Simultaneously, the 9-bit stored data is checked by the parity checker.

Guaranteed Operating Conditions

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4	6	pF
Output pin capacitance	C_{OUT}		6	8	pF

DC Characteristics

(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, unless otherwise noted.)

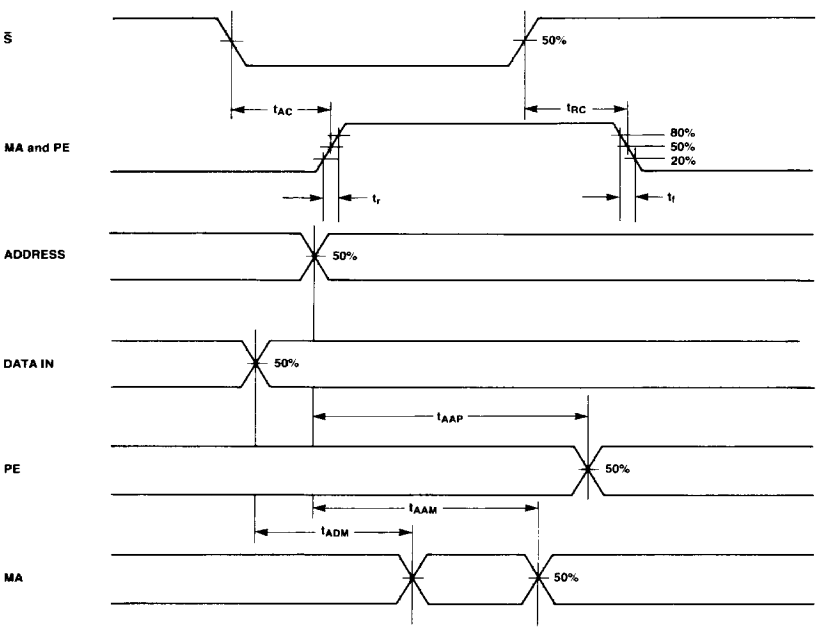
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output high voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output low voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output high voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output low voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input high current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input low current (V_{IN} = $V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{S}$ and PC/I Input low current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and outputs open)	I_{EE}	−260			mA	0°C to 75°C

AC Characteristics
(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥2.5 m/s unless otherwise noted.)

Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Parity error address access time	t_{AAP}	4	18	20	ns
Match address access time	t_{AAM}	4	18	20	ns
Match data in access time	t_{ADM}	2	12	15	ns
Chip select access time	t_{AC}	2	6	10	ns
Chip select recovery time	t_{RC}	2	6	10	ns

Read Cycle Timing Diagram

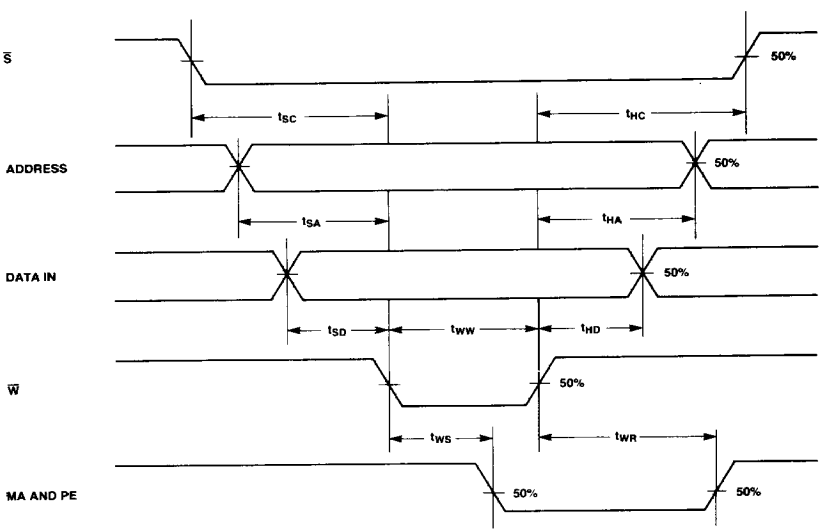


AC Characteristics
(Continued)
(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥2.5 m/s unless otherwise noted.)

Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse width	t_{WW}	17			ns
Write disable time	t_{WS}			10	ns
Write recovery time	t_{WR}			18	ns
Address set up time	t_{SA}	1.5			ns
Chip select set up time	t_{SC}	1.5			ns
Data set up time	t_{SD}	1.5			ns
Address hold time	t_{HA}	1.5			ns
Chip select hold time	t_{HC}	1.5			ns
Data hold time	t_{HD}	1.5			ns

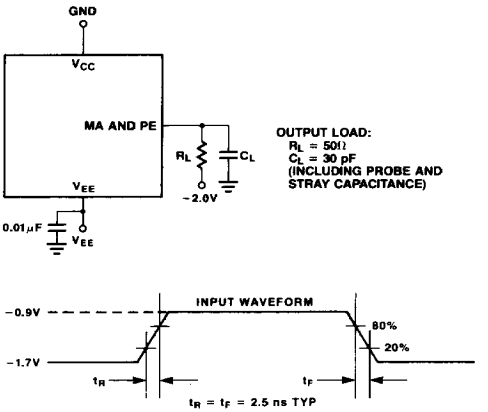
Write Cycle Timing Diagram



Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r	1.0	2.0	5.0	ns
Output fall time	t_f	1.0	2.0	5.0	ns

AC Test Conditions



NOTE: ALL TIMING MEASUREMENTS REFERENCED 50% INPUT LEVELS.