


**FUJITSU**

# ECL COLOR GRAPHIC PALETTE

**MB70805**

 May 1988  
Edition 1.0

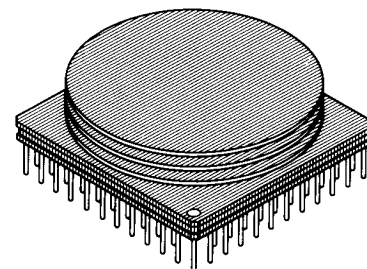
## 8196-BIT ECL COLOR GRAPHIC PALETTE MEMORY

The Fujitsu MB70805 is an ECL color graphic palette memory designed for graphic display applications. This device is organized as 1024 words by 4 bits by 2 planes look-up-table, 64 words by 6 bit mixing RAM, and equivalent 900 gates logic circuits. It features on chip voltage compensation for improved noise margin.

Operation for the MB70805 is specified over an ambient temperature range of from 0°C to 70°C (TA). It is packaged in 80-pin ceramic PGA, and fully compatible with industry standard 10K series ECL families.

Graphic data goes through the shift register where two phases graphic data is output to the look-up-table as the serialized 10-bit address inputs. Graphic data, character data, and cursor are edited in the high speed mixing circuits. Priority of these data is determined by writing the blightness data into the mixing RAM. Also, embedded CRC circuits enables real time scanning of mixing RAM output data.

- Equivalent gate count: 900 gates
- Look-Up-Table: 1024 words by 4 bits by 2 planes
- Mixing RAM: 64 words by 6 bits
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10K series ECL families
- 1024 colors can be displayed at a time
- Maximum frequency: 125MHz
- LUT Address access time: 18ns max
- Address data setup time: 15ns max
- Write pulse width: 15ns min
- MIX-RAM
- Address access time: 18ns max
- Address data setup time: 15ns min
- Write pulse width: 15ns min
- Power dissipation: 5.2W typ.
- DOPOS and IOP-II processing
- 80-pin ceramic PGA (Suffix: CR)  
(PGA-80C-A01)

**ADVANCE  
INFORMATION**

**CERAMIC PACKAGE  
PGA-80C-A01**

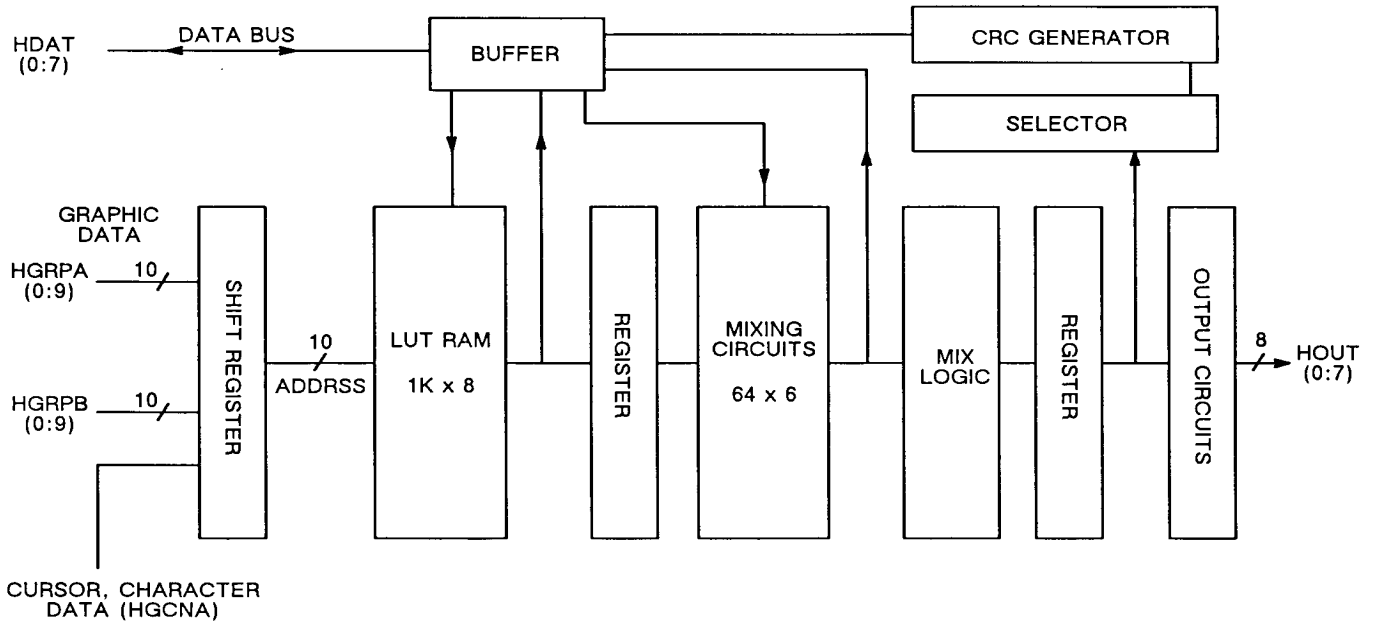
### ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VEE Pin Potential to Ground Pin	VEE	+0.5 to -7.0	V
Input Voltage	V <sub>IN</sub>	+0.5 to -4.0	V
Output Current (DC, Output High)	I <sub>OUT</sub>	-30	mA
Temperature under Bias	T <sub>C</sub>	-55 to +90	°C
Storage Temperature	T <sub>STG</sub>	-40 to +125	°C

**NOTE:** Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

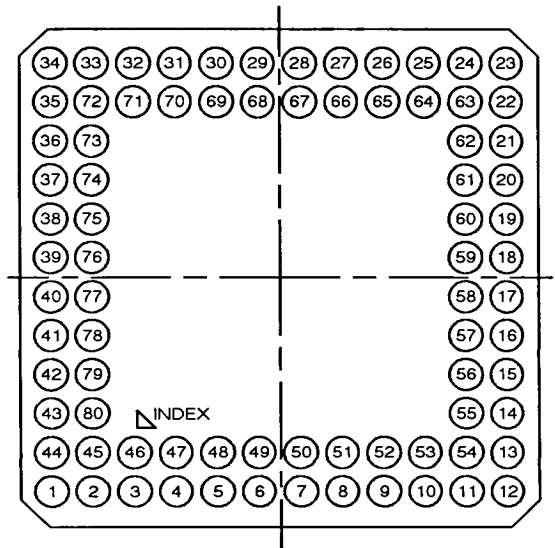
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

BLOCK DIAGRAM



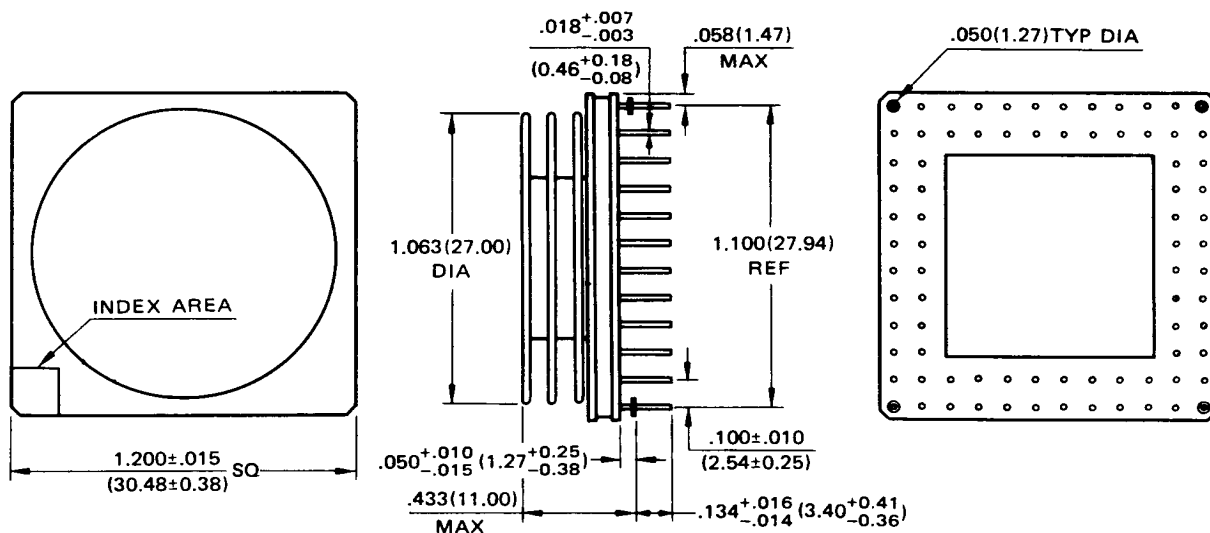
PIN ASSIGNMENT

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Vcc	31	HGRPA3	61	HGCNB3
2	HDATA1	32	HGRPA2	62	NGRPB9
3	HDATA2	33	HGRPBI	63	VEE
4	HDATA4	34	Vcc	64	HGRPBI8
5	HDATA5	35	HGRPBO	65	HGRPA7
6	HDATA7	36	HGCNA4	66	HGRPBI5
7	HOUT0	37	HGCNA2	67	Vcc
8	HOUT2	38	HGCNA1	68	Vcc
9	HOUT3	39	LLOAD0	69	HGRPA4
10	HOUT5	40	HVDISP	70	HGRPBI2
11	HOUT6	41	HTEST3	71	HGRPA1
12	Vcc	42	HTEST2	72	VEE
13	CKOUT	43	HCRC2	73	HGRPA0
14	HRLW	44	HCRC0	74	HGCNA3
15	HINT1	45	VEE	75	HGCNA0
16	HINT0	46	HDATA0	76	LLOAD1
17	HCLOCK	47	HDATA3	77	VEE
18	HMRAD0	48	HDATA6	78	HTEST4
19	HGCNB1	49	Vcc	79	HTEST1
20	NGCNB2	50	Vcc	80	HCRC
21	HGCNB4	51	HOUT1		
22	HGRPA9	52	HOUT4		
23	Vcc	53	HOUT7		
24	HGRPA8	54	VEE		
25	HGRPBI7	55	LCE		
26	HGRPBI6	56	LSTR		
27	HGRPA6	57	HGMASK		
28	HGRPA5	58	HMRAD1		
29	HGRPBI4	59	VEE		
30	HGRPBI3	60	HGCNB0		



# PACKAGE DIMENSIONS

80-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE  
(CASE No.: PGA-80C-A01)



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Dimensions in inches (millimeters)

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