



MOTOROLA

MC3245

QUAD TTL TO MOS DRIVER

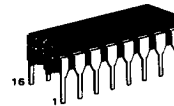
This high-speed driver is intended as a clock (high-level) driver for 22-pin and 18-pin dynamic NMOS RAMs and CCD memories. It is designed to operate on nominal +5 V and +12 V power supplies.

The channel control logic is organized so that all four drivers may be deactivated for STANDBY operation, or single driver may be activated for READ/WRITE operation or all four drivers may be activated for REFRESH operation.

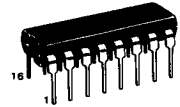
- Control Logic Optimized for Use in MOS RAM Systems
- Output Voltages Compatible with Many Popular MOS RAMs
- TTL and DTL Compatible Inputs — High-Speed Switching
- Interchangeable with Intel 3245

**GATE-CONTROLLED
FOUR-CHANNEL
MOS CLOCK DRIVERS**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

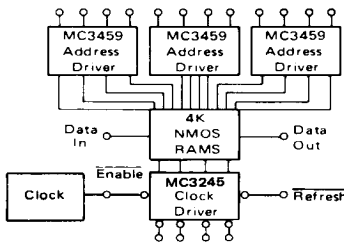


**L SUFFIX
CERAMIC PACKAGE
CASE 620**

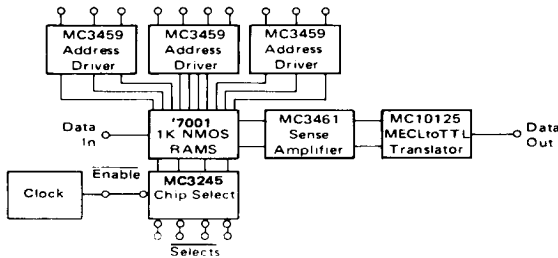


**P SUFFIX
PLASTIC PACKAGE
CASE 648**

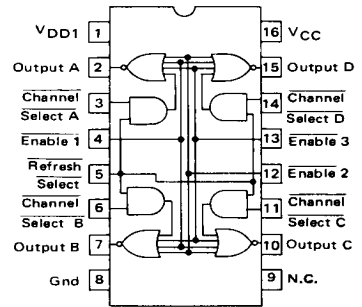
TYPICAL APPLICATION WITH 4K NMOS RAM IN TTL SYSTEM



TYPICAL APPLICATION WITH '7001 RAM AND TTL SYSTEMS



PIN CONNECTIONS



TRUTH TABLE

Inputs					Output
Control			Address		
Enable 1	Enable 2	Enable 3	Channel Select	Refresh Select	Output
H	H	I	I	I	L
I	I	H	I	I	L
I	I	I	H	H	L
L	L	L	L	I	H
L	L	L	I	L	H

H = High Logic State
L = Low Logic State
I = Irrelevant

MAXIMUM RATINGS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}	-0.5 to +7.0	Vdc
	V_{DD}	-0.5 to +14	Vdc
Output Voltage	V_O	-1.0 to $V_{DD} + 1.0$	Vdc
Input Voltage	V_I	-1.0 to V_{DD}	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Junction Temperature	T_J	Ceramic Package	175
		Plastic Package	150

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
Operating Ambient Temperature Range	T_A	0	-	75	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature conditions. Typical values measured at $T_A = 25^{\circ}\text{C}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage – High Logic State ($V_{IL} = 0.8\text{ V}$, $I_{OH} = -1.0\text{ mA}$)	V_{OH}	$V_{DD} - 0.5$	-	-	Vdc
Output Clamp Voltage – High Logic State ($I_{OH} = 5.0\text{ mA}$, $V_{IL} = 0\text{ V}$)	V_{OHC}	-	-	$V_{DD} + 1.0$	Vdc
Output Voltage – Low Logic State ($V_{IH} = 2.0\text{ V}$, $I_{OL} = 5.0\text{ mA}$)	V_{OL}	-	-	0.45	Vdc
Output Clamp Voltage – Low Logic State ($V_{IH} = 5.0\text{ V}$, $I_{OL} = -5.0\text{ mA}$)	V_{OLC}	-1.0	-	-	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	-	-	Vdc
Input Voltage – Low Logic State	V_{IL}	-	-	0.8	Vdc
Input Clamp Voltage ($I_{IK} = -5.0\text{ mA}$)	V_{IK}	-	-	-1.0	Vdc
Input Current – High Logic State ($V_I = 5.0\text{ V}$) Channel Select Inputs Refresh Select and Enable Inputs	I_{IH}	-	-	10 40	μA
Input Current – Low Logic State ($V_{IL} = 0.45\text{ V}$) Channel Select Inputs Refresh Select and Enable Inputs	I_{IL}	-	-	-0.25 -1.0	mA
Power Supply Current – Output High Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IL} = 0\text{ V}$, $I_{OH} = 0\text{ mA}$, $V_{DD} = 12.6\text{ V}$)	I_{CCH}	-	23	30	mA
	I_{DDH}	-	19	26	mA
Power Supply Current – Output Low Logic State ($V_{CC} = 5.25\text{ V}$, $V_{IH} = 5.0\text{ V}$, $I_{OL} = 0\text{ mA}$, $V_{DD} = 12.6\text{ V}$)	I_{CCL}	-	29	39	mA
	I_{DDL}	-	12	15	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature conditions. Typical values measured at +25°C.)

Characteristic	Symbol	Min (1)	Typ (2)	Max (3)	Unit
Delay Time					ns
Output High to Low Level ($R_S = 0 \Omega$)	t_{DHL}	3.0	7.0	—	
Output Low to High Level ($R_S = 0 \Omega$)	t_{DLH}	5.0	11	—	
Transition Time					ns
Output High to Low Level ($R_S = 20 \Omega$)	t_{THL}	5.0	17	25	
Output Low to High Level ($R_S = 20 \Omega$)	t_{TLH}	10	17	25	
Propagation Delay Time					ns
Output High to Low Level ($R_S = 0 \Omega$)	t_{PHL}	—	18	32	
Output Low to High Level ($R_S = 0 \Omega$)	t_{PLH1}	—	20	32	
($R_S = 20 \Omega$)	t_{PLH2}	—	27	38	

- (1) $C_L = 150 \text{ pF}$
- (2) $C_L = 200 \text{ pF}$
- (3) $C_L = 250 \text{ pF}$

CAPACITANCE* (Unless otherwise specified, $T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$, $V_I = 2.0 \text{ V}$, and $V_{CC} = 0 \text{ V}$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance					pF
Channel Select Inputs	$C_{in}(CS)$	—	5.0	8.0	
Input Capacitance					pF
Refresh or Enable Inputs	$C_{in}(\bar{E})$	—	8.0	12	

*Periodically sampled, but not 100% tested.

FIGURE 1 – SWITCHING TEST WAVEFORMS

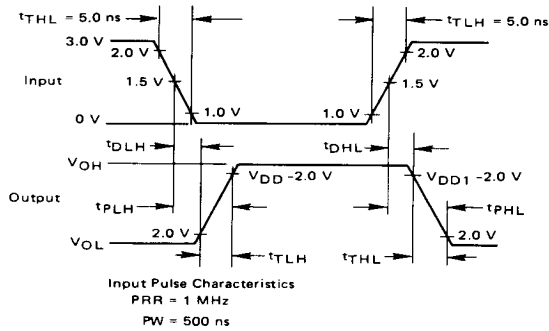


FIGURE 2 – SWITCHING TEST CIRCUIT

