MOTOROLA

MCM2167H

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

16,384-BIT STATIC RANDOM ACCESS MEMORY

SRAM

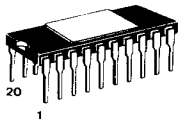
FAST 16K BIT STATIC RAM

The MCM2167H is a 16,384-bit Static Random Access Memory organized as 16,384 words by 1 bit, fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are no longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications demanding superior performance and reliability.

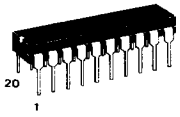
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after Chip Enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as the Chip Enable ($\overline{E}$) remains high. This feature provides significant system-level power savings.

The MCM2167H is in a 20 pin dual-in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

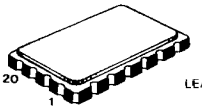
- Single +5 V Operation (±10%)
- Fully Static Memory — No Clock or Timing Strobe Required
- Fast Access Time: MCM2167H-35 — 35 ns Max.
  MCM2167H-45 — 45 ns Max.
  MCM2167H-55 — 55 ns Max.
- Power Dissipation: 120 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output



L SUFFIX
CERAMIC PACKAGE
CASE 729

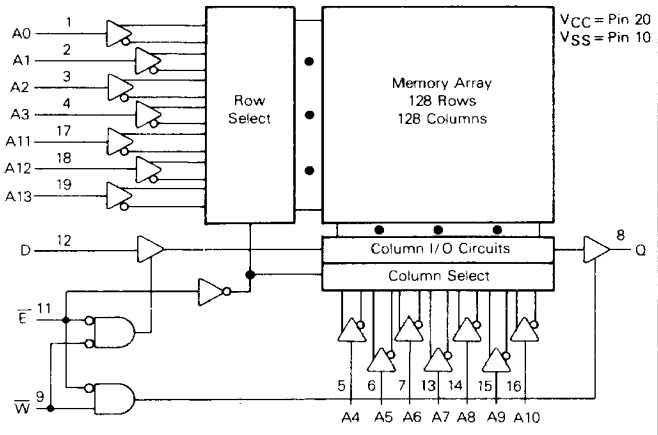


P SUFFIX
PLASTIC PACKAGE
CASE 738

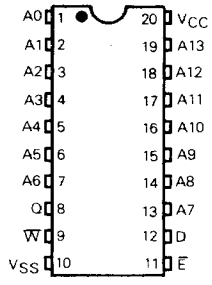


Z SUFFIX
LEADLESS CHIP CARRIER
CASE 752B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A13	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−0.5 to +7.0	V
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage* *	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

**50 ns maximum address rise and fall times, while the chip is selected.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{E} = V_{IH}$, $V_{I/O}$ = GND to V_{CC}, V_{CC} = 5.5 V)	I_{LO}	−50	50	μA
Operating Power Supply Current ($\overline{E} = V_{IL}$, $I_{I/O}$ = 0 mA)	I_{CC1}	–	120	mA
Standby Power Supply Current ($\overline{E} = V_{IH}$)	I_{SB}	–	20	mA
Output Low Voltage (I_{OL} = 8.0 mA) See Figure 1	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA) See Figure 1	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance except, $\overline{E}$, DQ	C_{in}	3	5	pF
Input/Output Capacitance and $\overline{E}$ Input Capacitance	$C_{I/O}$	3	7	pF

MODE SELECTION

Mode	$\overline{E}$	$\overline{W}$	V_{CC} Current	Q
Standby	H	X	I_{SB}	High Z
Read	L	H	I_{CC}	Data Out
Write Cycle (1)	L	L	I_{CC}	High Z
Write Cycle (2)	L	L	I_{CC}	High Z

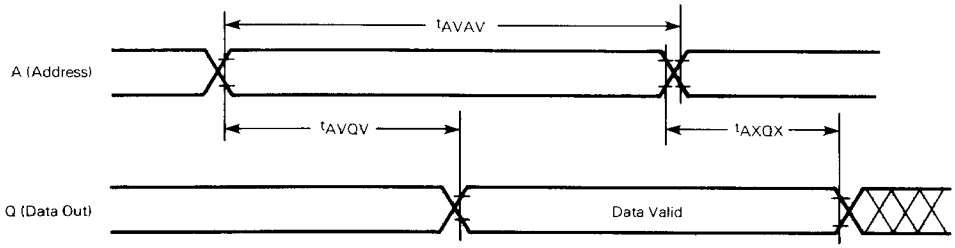
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

Input Pulse Levels . . . . . 0 and 3.0 Volts
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Reference Levels . . . . . 0.8 and 2.0 Volts
Output Load . . . . . See Figure 2

READ CYCLE #1 (Address Controlled) $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AA}	–	35	–	45	–	55	ns
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	35	–	45	–	55	–	ns
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	3	–	3	–	3	–	ns

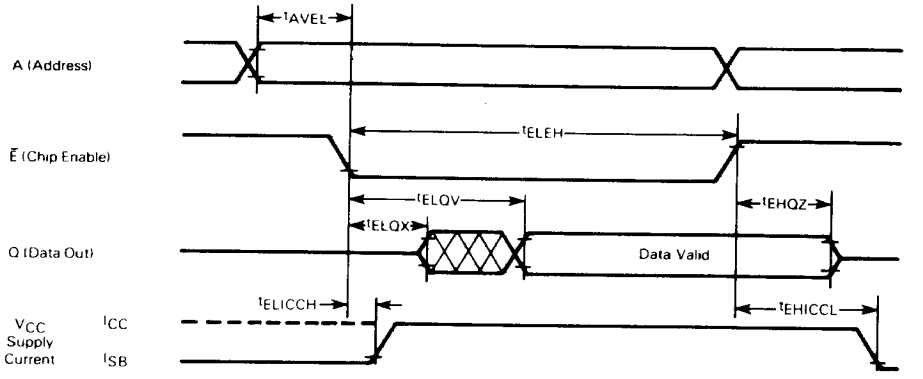


SRAM

READ CYCLE #2 (Chip Enable Controlled) Notes 1 and 2

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	35	–	45	–	55	ns
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	35	–	45	–	55	–	ns
Address Valid to Chip Enable Low (Address Setup to Enable Active)	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{LZ}	5	–	5	–	5	–	ns
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{HZ}	0	25	0	25	0	30	ns
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	35	–	45	–	55	ns

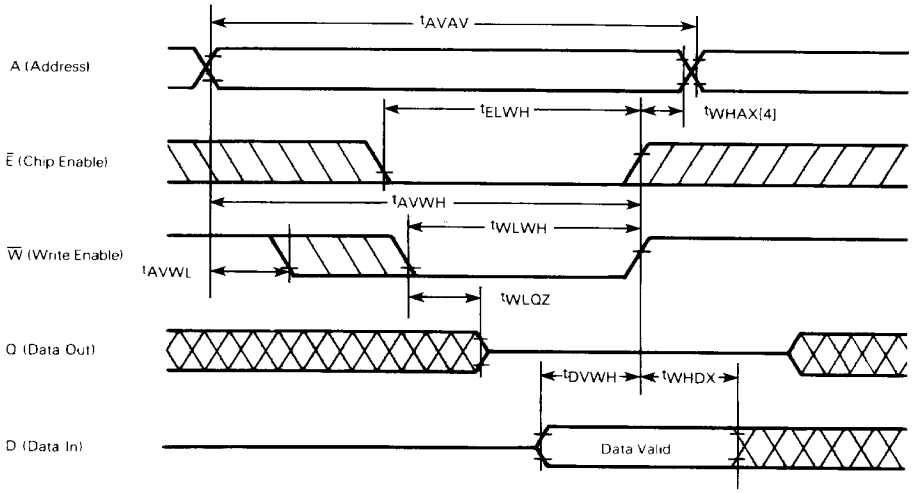
NOTES:
1. Write Enable ($\overline{W}$) is high for read cycle.
2. Address valid prior to or coincident with Chip Enable ($\overline{E}$) transition low.



WRITE CYCLE #1 (Write Controlled) Note 3

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	–	45	–	55	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	20	–	20	–	25	–	ns
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	35	–	45	–	55	–	ns
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DW}	15	–	15	–	20	–	ns
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	–	0	–	0	–	ns
Address Valid to Write High (Address Setup to End of Write)	t_{AVWH}	t_{AW}	35	–	45	–	55	–	ns
Address Valid to Write Low (Address Setup to Beginning of Write)	t_{AVWL}	t_{AS}	5	–	5	–	10	–	ns
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WZ}	0	20	0	20	0	25	ns
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{OW}	0	25	0	25	0	30	ns

NOTES:
3. Either Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) must be high during all address transitions.
4. t_{WHAX} is measured from the earlier of Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) going high to the end of write cycle.



WRITE CYCLE #2 (Chip Enable Controlled) Note 5

Parameter	Symbol		MCM2167H-35		MCM2167H-45		MCM2167H-55		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	–	45	–	55	–	ns
Write Low to Chip Enable High (Write Pulse Width)	t_{WLEH}	t_{WP}	20	–	20	–	20	–	ns
Chip Enable Low to Chip Enable High (Chip Enable to End of Write)	t_{ELEH}	t_{EW}	35	–	45	–	55	–	ns
Data Valid to Chip Enable High (Data Setup to End of Write)	t_{DVEH}	t_{DW}	15	–	15	–	20	–	ns
Chip Enable High to Data Don't Care (Data Hold After End of Write)	t_{EHDX}	t_{DH}	5	–	5	–	5	–	ns
Address Valid to Chip Enable High (Address Setup to End of Write)	t_{AVEH}	t_{AW}	35	–	45	–	55	–	ns
Chip Enable High to Address Don't Care (Address Hold After End of Write)	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns

NOTES:
5. Either Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) must be high during all address transitions.
6. t_{EHAX} is measured from the earlier of Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) going high to the end of write cycle.

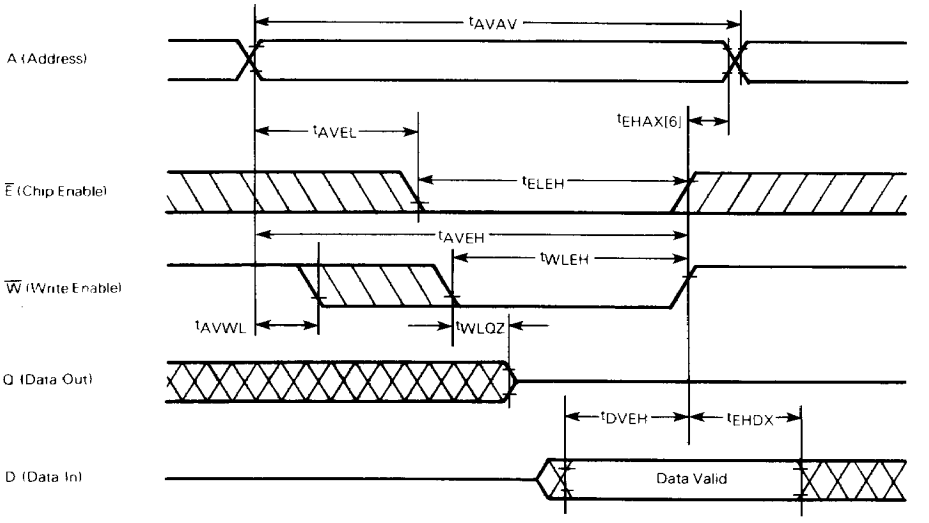


FIGURE 1 — DC OUTPUT LOAD

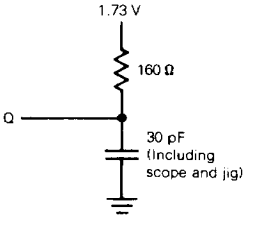


FIGURE 2 — AC OUTPUT LOAD