DRAM

1MEG x 1 DRAM

NIBBLE MODE

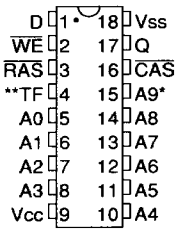
FEATURES

- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Nibble Mode access cycle

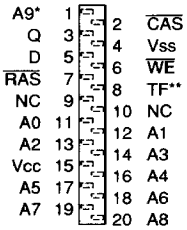
OPTIONS	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

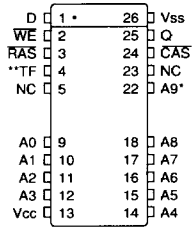
20 Pin DIP (PD, CD)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)



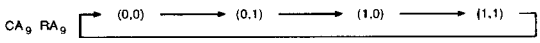
*Address not used for $\overline{RAS}$ ONLY refresh
**TF = Test Function, V_{IN} must be disconnected or between Vss and Vcc for normal operation.

GENERAL DESCRIPTION

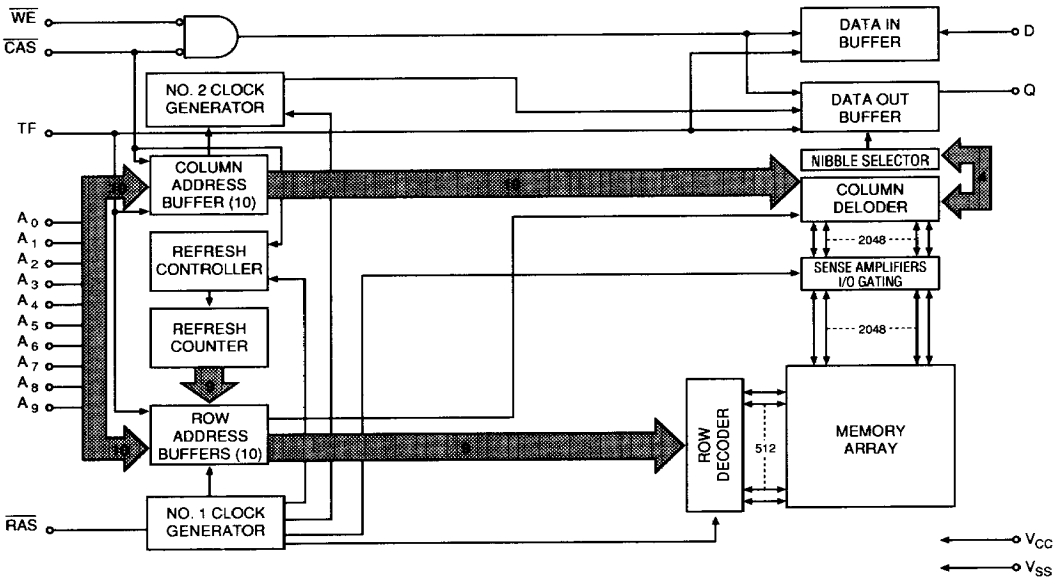
The MT4C1025 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

NIBBLE MODE operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and $\overline{RAS}$ address A9 (nibble LSB) selecting one of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM
NIBBLE MODE



TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	X	High Impedance
READ	L	L	H	X	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
NIBBLE READ	L	H→L→H	H	X	ROW	COL	Valid Data Out, Valid Data Out
NIBBLE WRITE	L	H→L→H	L	X	ROW	COL	Valid Data In, Valid Data In
NIBBLE READ-WRITE	L	H→L→H	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	X	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA) Output Low voltage (I_{OUT} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	70	60	50	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}	3	2	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}	1	1	1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	70	60	50	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	70	60	50	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	150		180		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	175		210		255		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{RAS}$ precharge time	t_{RP}	60		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	10	75	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		15		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	15	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		75		110		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	60		75		80		ns	
Write command pulse width	t_{WP}	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

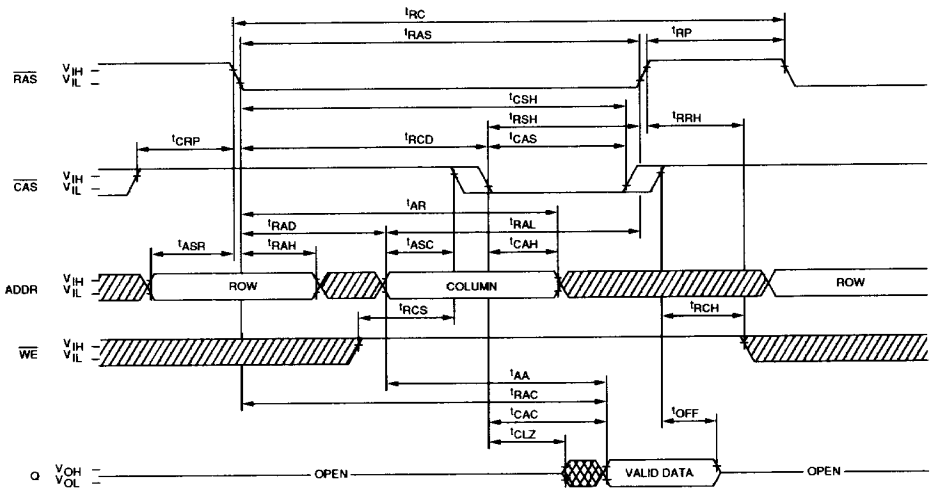
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		10		15		ns	
NIBBLE MODE cycle time	^tNC	40		45		55		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWC	65		75		85		ns	
NIBBLE MODE access time	^tNCAC		20		20		35	ns	15
NIBBLE MODE pulse width	^tNCAS	20		25		35		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		10		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	20		25		30		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WE}$ delay time	^tNCWD	20		25		35		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{RAS}$ lead time	^tNRWL	20		25		30		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{CAS}$ lead time	^tNCWL	20		25		30		ns	

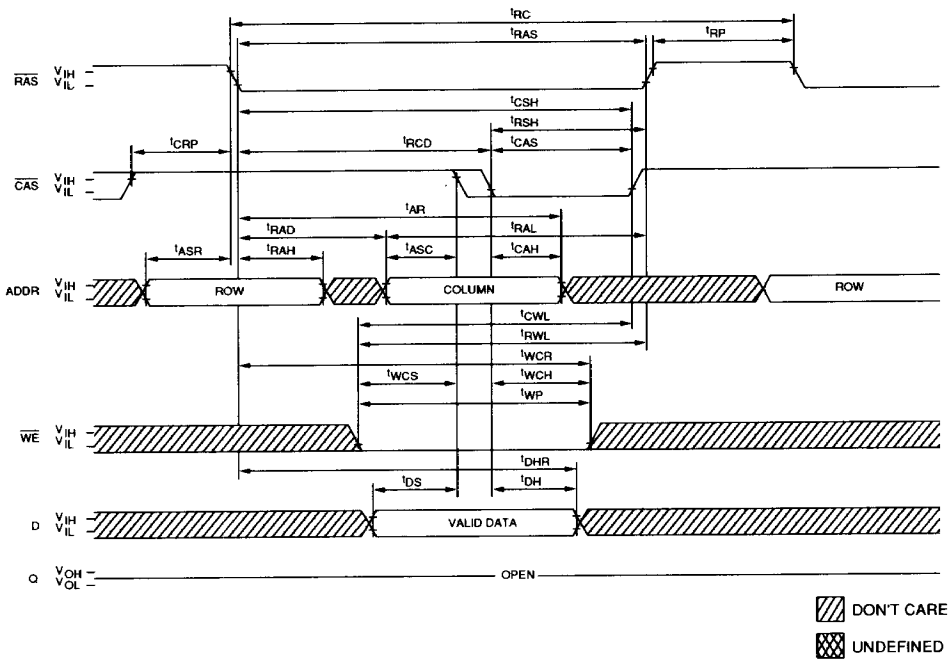
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

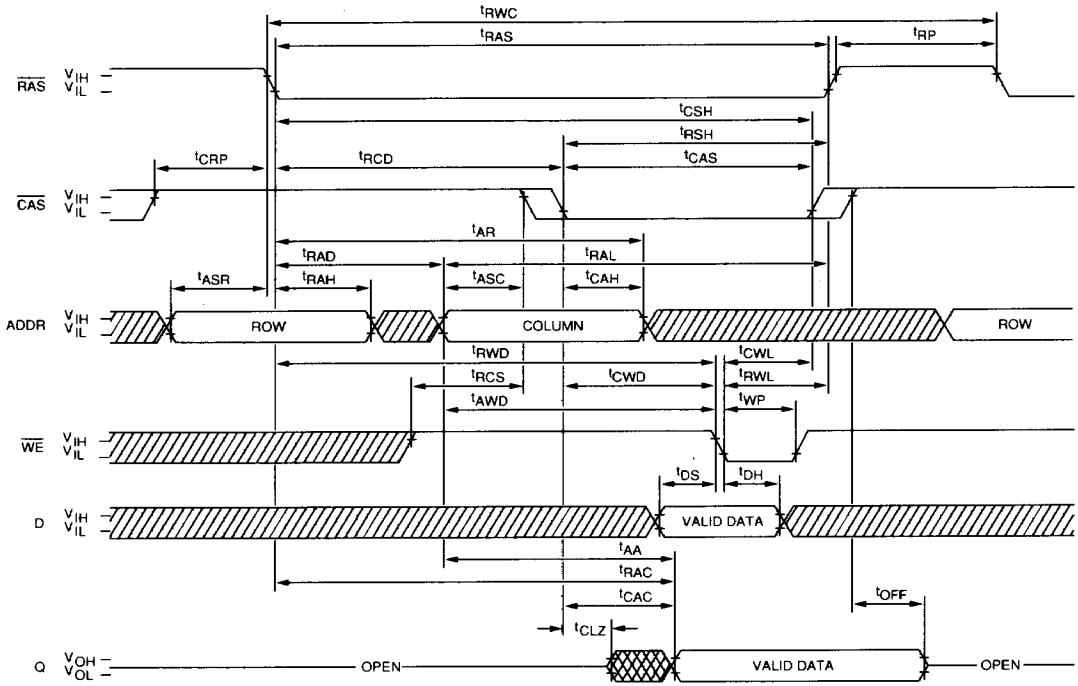
READ CYCLE



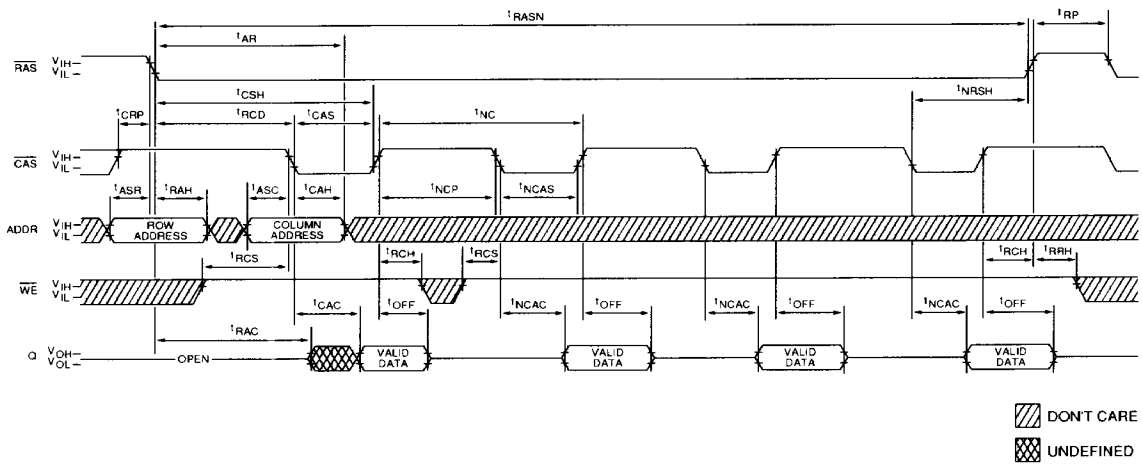
EARLY-WRITE CYCLE



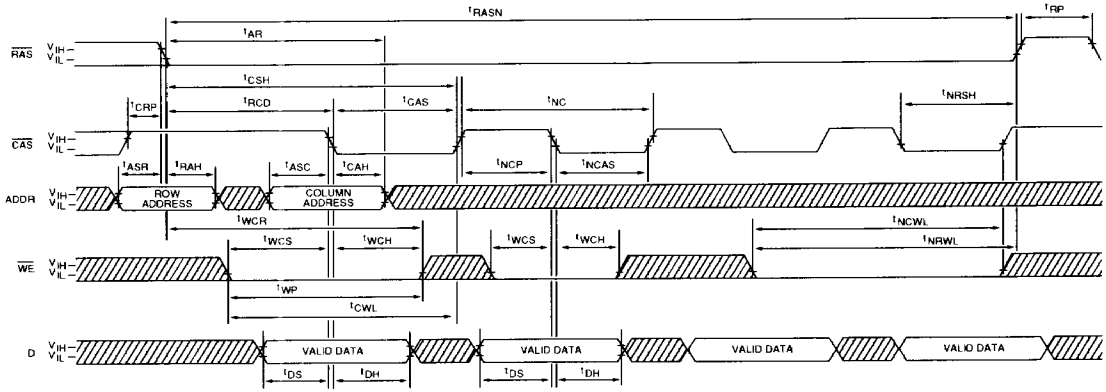
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



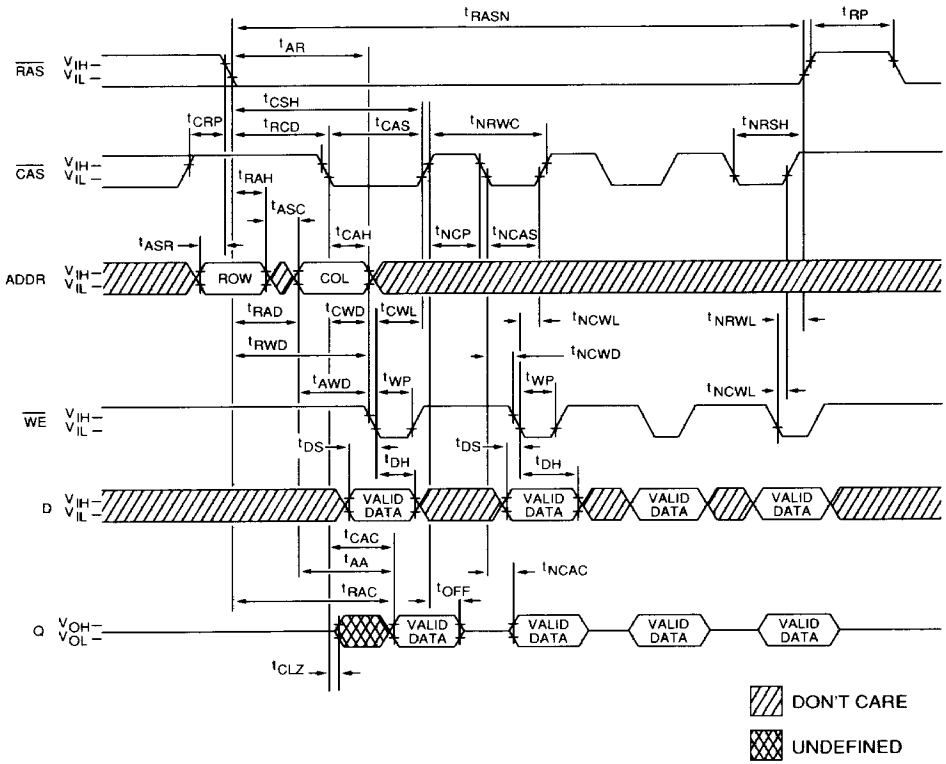
NIBBLE MODE READ CYCLE



NIBBLE MODE EARLY-WRITE CYCLE

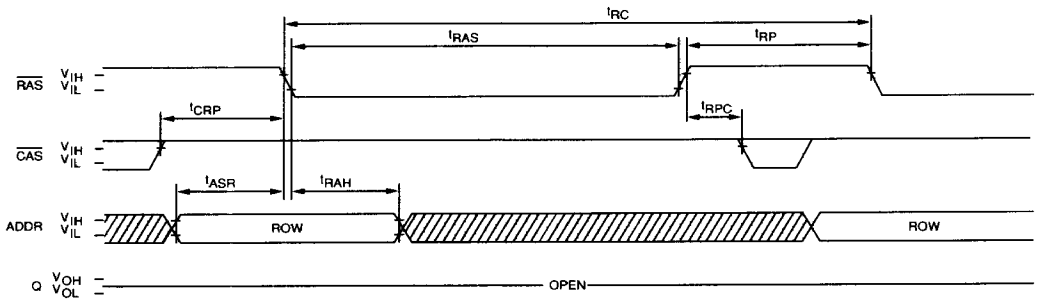


NIBBLE MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



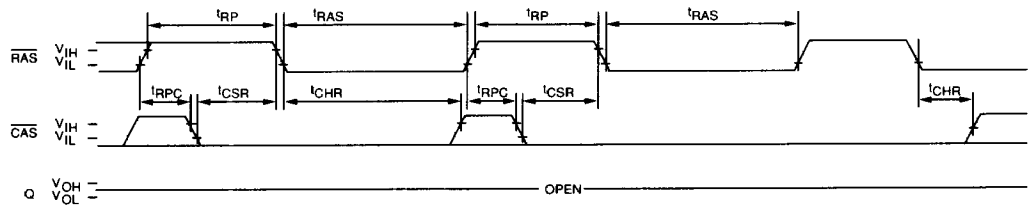
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]