2606-F,I,N • 2606-1-F,I,N

B = N

DESCRIPTION

The 2606 is fabricated with n-channel silicon gate MOS technology and achieves an access time of less than 750ns.

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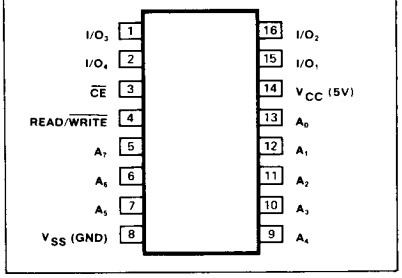
FEATURES

- **Fully decoded**
- **No clocks required**
- **All interface signals, including power supply directly TTL compatible**

PIN CONFIGURATION

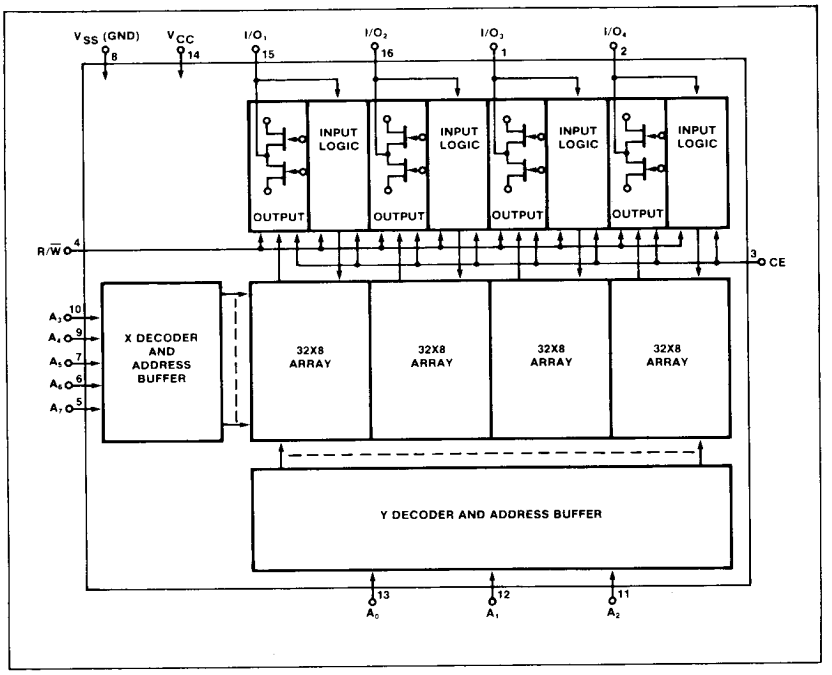
F,I,N PACKAGE



Tri-State per SIG.

2606-1F,I,N
2606F,I,N,B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ[2]	Max	
Input voltage					V
V_{IL} Low		-0.5		0.65	
V_{IH} High		2.2		V_{CC}	
Output voltage					V
V_{OL} Low	I_{OL} = 1.9mA			0.45	
V_{OH} High	I_{OH} = -100μA	2.4			
I_{LI} Input current	V_{IN} = 0 to 5.25V			10	μA
I/O leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}	$V_{I/O}$ = 4.0V			10	
I_{LOL}	$V_{I/O}$ = 0.45V			-100	
Supply current	V_{IN} = 5.25V, $I_{I/O}$ = OmA				mA
I_{CC1}	T_A = 25°C			70	
I_{CC2}	T_A = 0°C			80	
Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN} Input (All pins)	V_{IN} = OV		4	7	
$C_{I/O}$ I/O	V_{OUT} =OV		7	10	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C, V_{CC} = 5V ± 5% unless other specified.[4,5,6,7]

PARAMETER	TO	FROM	2606			2606-1			UNIT
			Min	Typ	Max	Min	Typ	Max	
READ CYCLE									
t_R Read cycle time			750		750	500		500	ns
t_A Access time									ns
T_{RO}[8]	Output enable	Read	100			75			ns
t_{CO}[8]	Output enable	Chip enable	0			0			ns
Previous data valid with respect to									ns
t_{VC} Chip disable			0		150	0		100	
t_{VA} Address change			50			50			
t_{CV} Delay time	Data valid	Chip enable			400			300	ns
t_{RC}	Chip enable	Read	100			50			ns
WRITE CYCLE A									
t_W Write cycle time	Write	Address	750			500			ns
t_{AW}			250			150			ns
t_{WW} Write pulse width			400			300			ns
t_{WR} Write recovery time			100			50			ns
Setup and hold time									ns
t_{CS} Setup time	R/W	Chip enable	0			0			
t_{CH} Hold time	Chip enable	R/W							
t_{DS} Setup time	R/W	Data	380			280			
t_{DH} Hold time[9]	Data	R/W	0			0			
t_{WD} Disable delay[10]	Data out	Write			125			100	ns
WRITE CYCLE B									
t_W Write cycle time	Chip enable	Address	750			500			ns
t_{AC}			250			150			ns
t_{CW} Chip enable pulse width			400			300			ns
t_{CR} Chip enable recovery time			100			50			ns
Setup and hold time[11]									ns
t_{WS} Setup time	Chip enable	R/W	200			100			
t_{WH} Hold time	R/W	Chip enable	0			0			
t_{DS} Setup time	Chip enable	Data	380			280			
t_{DH} Hold time[8]	Data	Chip enable	0			0			

NOTES on following page.

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. Input levels swing between 0.65V and 2.2V.
5. Input signal transition times are 20ns.
6. Timing reference level is 1.5V.
7. Bus load is 100pF, 1 TTL tri-state output.
8. R/$\overline{W}$ must be high and CE must be low in order for output buffers to turn on.
9. Maximum t_{DH} governed by potential conflict with data out during next cycle.
10. The output buffers will turn off within the specified time after write mode is selected.
11. Write setup required to prevent data overlap. For write cycle B the R/$\overline{W}$ line will typically change with the addresses.

TIMING DIAGRAM