2680-F,I,N • 2680-1-F,I,N • 2680-2-F,I,N

DESCRIPTION

The 2680 incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

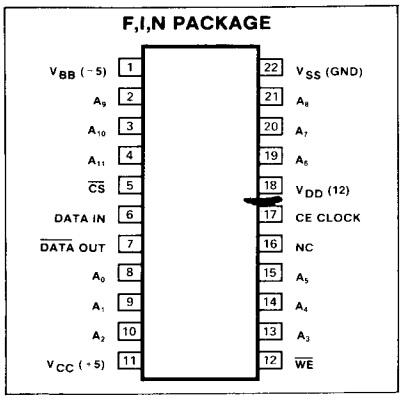
The 2680 must be refreshed every 2ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A_0-A_5). The chip select input can be either high or low for refresh.

The 2680 has been designed with minimum production costs as a prime criterion. It is fabricated using n-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The 2680 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance and low cost memory device.

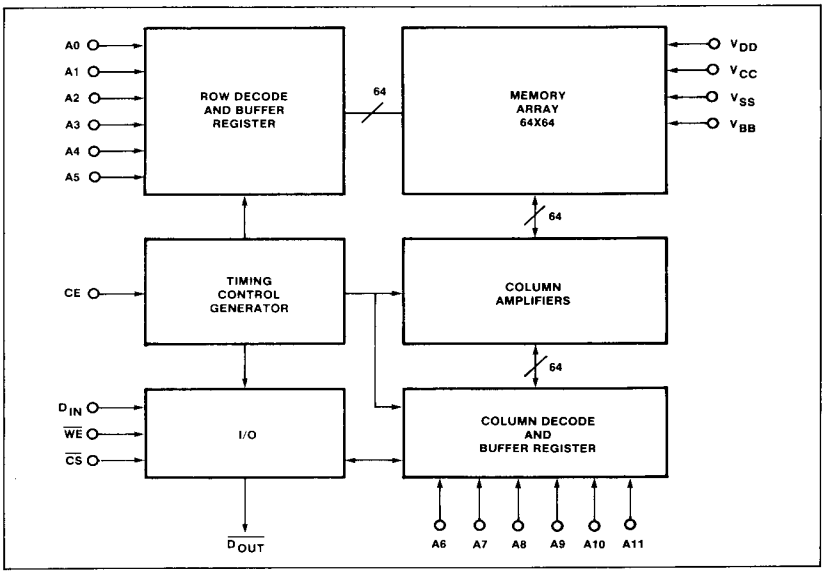
TRI-STATE

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1.25	W
	All input or output voltages with respect to the most negative supply voltage, V_{BB}	20 to -0.3	V
	Supply voltages V_{DD}, V_{CC}, and V_{SS} with respect to V_{BB}	20 to -0.3	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
Supply voltage				V
V_{CC}	4.75	5	5.25	
V_{DD}	11.4	12	12.6	
V_{SS}		0		
V_{BB}	-4.5	-5	-5.5	

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-1.0		0.6	
V_{IH}	High		2.4		V_{CC} +1	
V_{ILC}	CE low		-1.0		1.0	
V_{IHC}	CE high		V_{DD} -1		V_{DD} +1	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA	0.0		0.45	
V_{OH}	High	I_{OH} = -2.0mA	2.4		V_{CC}	
	Input load current					μA
I_{LC}	CE	V_{IN} = 0 min to V_{IHC} max		.01	2	
I_{LI}	All inputs except CE	V_{IN} = 0 min to V_{IH} max, CE = V_{ILC} or V_{IHC}		.01	10	
$\|I_{LO}\|$	Output leakage current high impedance state	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_0 = OV to 5.25V		.01	10	μA
	Supply current (V_{DD})					
I_{DD1}	During CE off[3]	CE = - 1V to 6V		50	200	μA
I_{DD2}	During CE on	CE = V_{IHC}, $\overline{CS}$ = V_{IL}			60	mA
I_{DDAV1}	Average V_{DD} current	Cycle time = 400ns, $\overline{CS}$ = V_{IL}, t_{CE} = 230ns, T_A = 25°C		35	54	mA
	Supply current					μA
I_{CC1}	V_{CC}[4]	CE = V_{ILC} or $\overline{CS}$ = V_{IH}		.01	10	
I_{BB}	V_{BB}			5	100	
	Capacitance[5]					pF
C_{AD}	Address, CS	V_{IN} = V_{SS}		4	6	
C_{CE}	CE	V_{IN} = V_{SS}		13	25	
C_{IN}	Input and $\overline{WE}$	V_{IN} = V_{SS}		5	10	
C_{OUT}	Output	V_{OUT} = OV		4	7	

AC ELECTRICAL CHARACTERISTICS

Over recommended supply voltage range, T_A = 0°C to 70°C, t_T = 20ns, C_L = 50pF, Load = 1 TTL gate, $t_{ACC} = t_{AC} + t_{CO} + 1t_T$

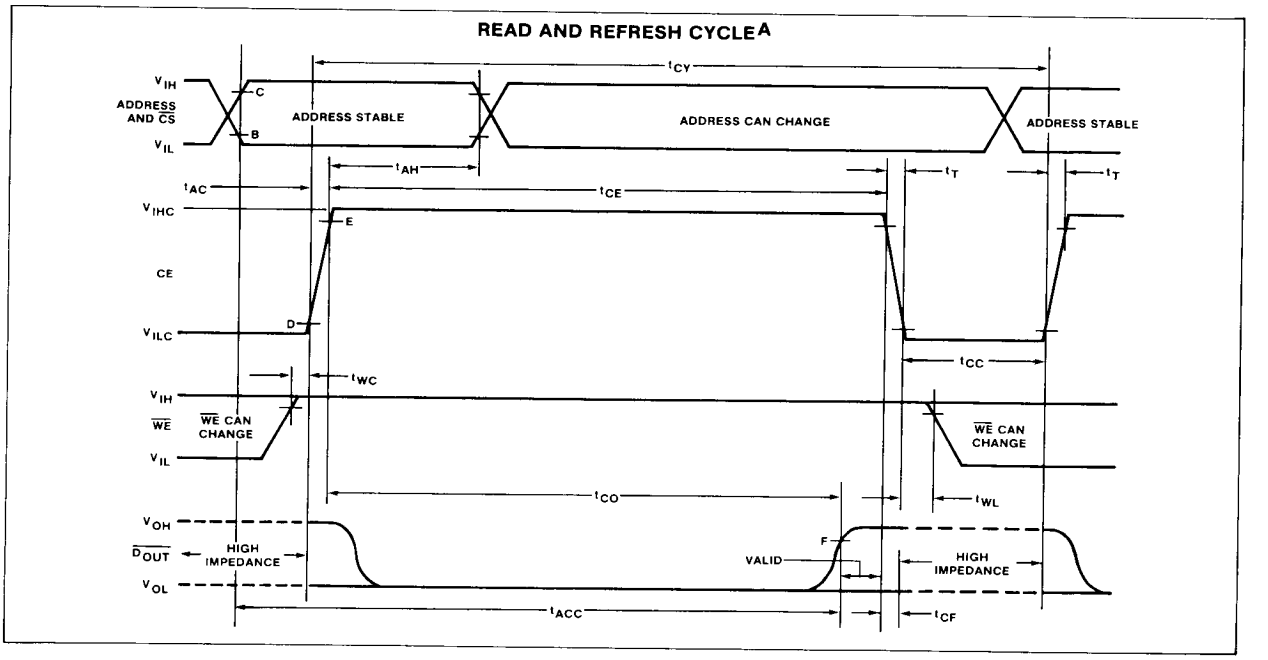
	PARAMETER	TO	FROM	2680			2680-1			2680-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ, WRITE, AND READ MODIFY/ WRITE CYCLE												
t_{REF}	Time between refresh					2			2			1	ms
	Setup and hold time												ns
t_{AC}	Setup time	CE	Address	0			0			10			
t_{AH}	Hold time	Address	CE	100			100			100			
t_{CC}	CE off time			130			130			380			ns
t_T	CE transition time			10		40	10		40	10		40	ns
t_{CF}	CE high impedance state	Output	CE off	0			0			0			ns
	READ CYCLE												
t_{CY}	Cycle time			400			470			800			ns
t_{CE}	CE on time			230		4000	300		4000	380		4000	ns
t_{CO}	CE output delay time					180			250			320	ns
t_{ACC}	Access time	Output	Address			200			270			350	ns
t_{WL}		$\overline{WE}$	CE	0			0			0			ns
t_{WC}		CE on	$\overline{WE}$	0			0			0			ns
	WRITE CYCLE												
t_{CY}	Cycle time			400			470			800			ns
t_{CE}	CE on time			230		4000	300		4000	380		4000	ns
t_W		CE off	$\overline{WE}$	150			150			200			ns
t_{CW}		$\overline{WE}$	CE	150			150			150			ns
	Setup and hold time												ns
t_{DW}	Setup time[6]	$\overline{WE}$	D_{IN}	0			0			0			
t_{DH}	Hold time	D_{IN}	CE	0			0			0			
	Pulse width												ns
t_{WP}	$\overline{WE}$			50			50			100			
	READ, MODIFY, WRITE CYCLE												
t_{RWC}	Cycle time			520			590			960			ns
t_{CRW}	CE width during cycle			350		4000	420		4000	540		4000	ns
t_W		CE off	$\overline{WE}$	150			150			200			ns
t_{WC}		CE on	$\overline{WE}$	0			0			0			ns
	Setup and hold time												ns
t_{DW}	Setup time	$\overline{WE}$	D_{IN}	0			0			0			
t_{DH}	Hold time	D_{IN}	CE	0			0			0			
	Pulse width												ns
t_{WP}	$\overline{WE}$			50			50			100			
t_{CO}	Delay time	Output	CE			180			250			320	ns
t_{ACC}	Access time					200			270			350	ns

NOTES

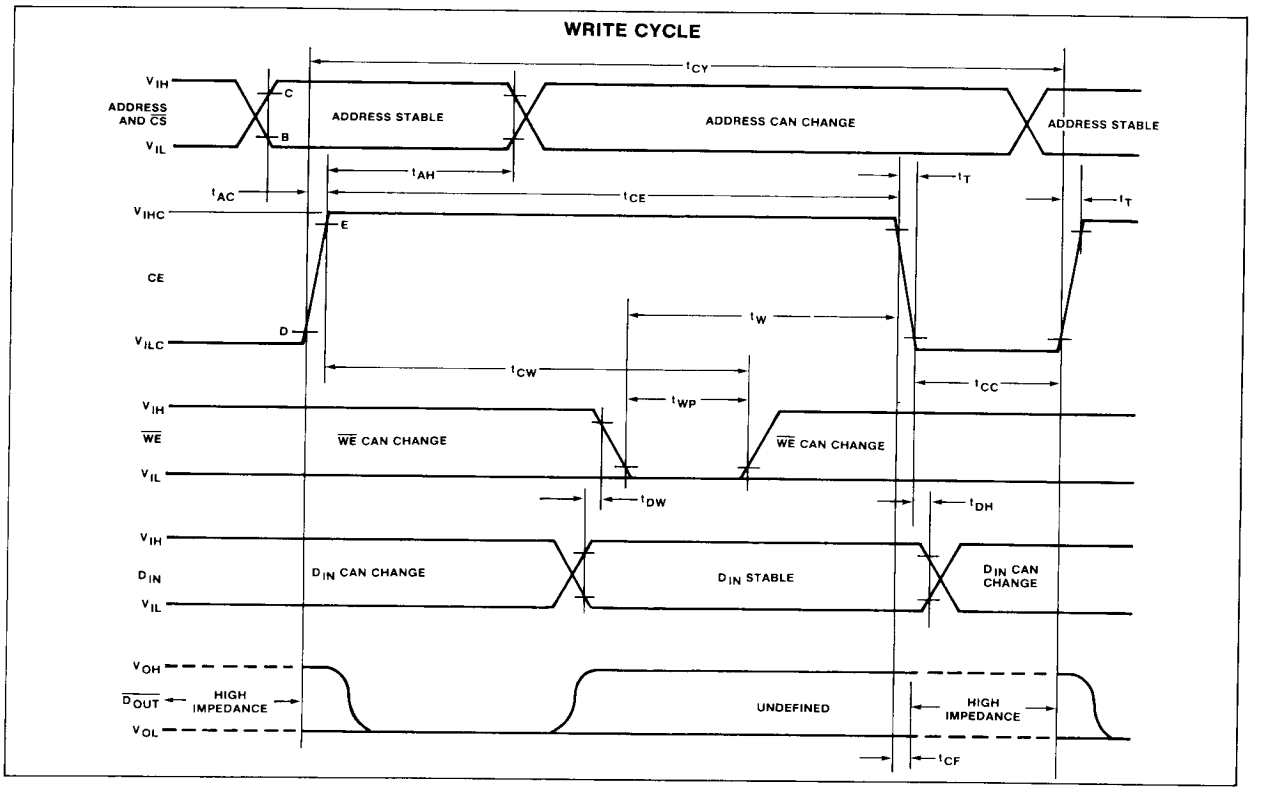
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading V_{CC} is connected to output buffer only.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation with the current equal to a constant 20mA.
6. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
7. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.

TIMING DIAGRAMS

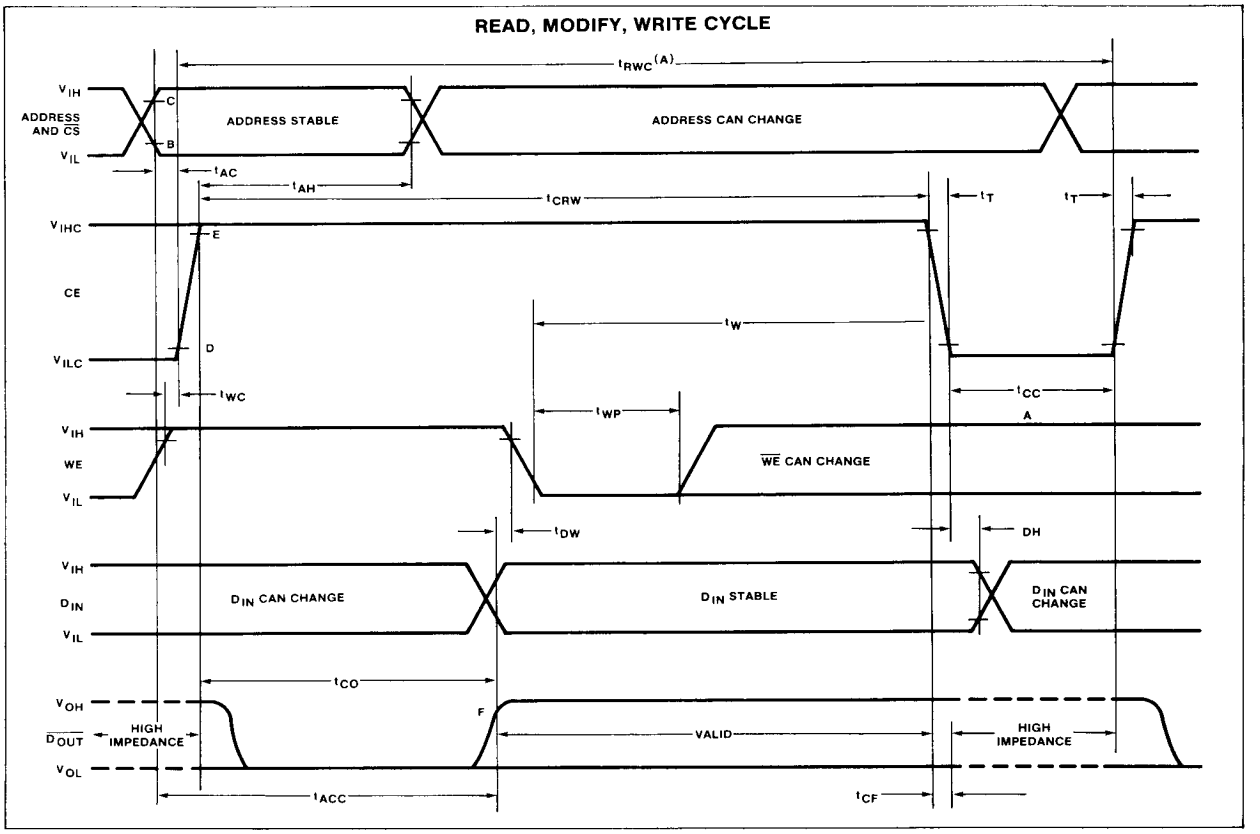
READ AND REFRESH CYCLE[A]



WRITE CYCLE



TIMING DIAGRAMS (Cont'd)



NOTES

A. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
B. V_{IL} max is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
C. V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
D. V_{SS} +2.0V is the reference level for measuring timing of CE.
E. V_{DD} -2V is the reference level for measuring timing of CE.
F. V_{SS} +2.4V is the reference level for measuring the timing of D_{OUT}.