

TDA2591/TDA2593 Line Oscillator Combination

General Description

The TDA2591 and TDA2593 are integrated line oscillator circuits for color television receivers using thyristor or transistor line deflection output stages.

Features

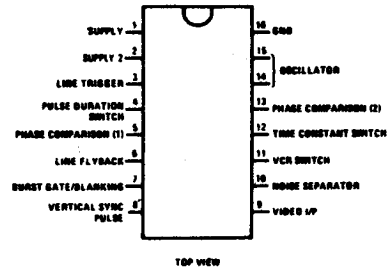
- Line oscillator based on the threshold switching principle
- Phase comparison between sync pulse and oscillator voltage
- Phase comparison between line flyback pulse and oscillator voltage
- Switch for changing the filter characteristic and the gate circuit (when used for VCR)
- Coincidence detector
- Sync separator
- Noise separator
- Vertical sync separator
- Color burst keying and line flyback blanking pulse generator
- Phase shifter for the output pulse
- Output pulse duration switching
- Output stage for direct drive of thyristor deflection circuits
- TDA2591 for use in combination with TDA2522 & TDA2560 PAL decoder.
- TDA2593 for use in combination with TDA3500 PAL decoder.

Reference Data

PARAMETERS		MIN	TYP	MAX	UNITS
V1-16	Supply Voltage		12		V
I_1	Supply Current		30		mA
Input Signals					
V9-16 (p-p)	Sync Separator Input Voltage (Peak-to-Peak Value)		3		V
V10-16 (p-p)	Noise Separator Input Voltage (Peak-to-Peak Value)		3		V
	Pulse Duration Switch Input Voltage				
V4-16	$t = 7 \mu s$	8.2		13.2	V
V4-16	$t = 14 \mu s + t_d$	0		4.0	V
V11-16	Voltage for Switching on VCR	9		12	V
		0		1.5	V
Output Signals					
V8-16 (p-p)	Vertical Sync Output Pulse (Peak-to-Peak Value)		11		V
V7-16 (p-p)	Burst Gating Output Pulse (Peak-to-Peak Value)		11		V
V3-16 (p-p)	Line Trigger Pulse (Peak-to-Peak Value)		10.5		V

Connection Diagram

Dual-In-Line Package



Dual-In-Line Package, Order Number TDA2591 or TDA2593
See NS Package N16A

Quad-In-Line Package, Order Number TDA2591Q or TDA2593Q
See NS Package N16C

Absolute Maximum Ratings

Voltages				
V1-16, Supply Voltage at Pin 1 (When Supplied by the IC)	13.2V	I ₄ , Pin 4 Current	1 mA	
V2-16, Supply Voltage at Pin 2	18V	I ₁₆ , Pin 6 Current	10 mA	
V4-16, Pin 4 Voltage	0 to 13.2V	I ₇ , Pin 7 Current	10 mA	
V9-16, Pin 9 Voltage	-6 to +6V	I ₁₁ , Pin 11 Current	2 mA	
V10-16, Pin 10 Voltage	-6 to +6V	Power Dissipation		
V11-16, Pin 11 Voltage	0 to 13.2V	P _{TOT} , Total Power Dissipation (Note 6)	800mW	
Currents		Temperatures		
I _{2M} , Pin 2 Current (Peak Value)	650 mA	T _{STG} , Storage Temperature	-25°C to +125°C	
I _{3M} , Pin 3 Current (Peak Value)	650 mA	T _A , Operating Ambient Temperature	-20° to +60°C	

Electrical Characteristics V1-16 = 12V; T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNITS
REQUIRED INPUT SIGNALS					
Sync Separator					
V9-16	Input Switching Voltage		0.8		V
I _g	Input Switching Current	5		100	μA
I _g	Input Blocking Current at V9-16 = -5V		<1		μA
Noise Separator					
V10-16	Input Keying Voltage		1.0		V
V10-16	Input Switching Voltage		1.4		V
I ₁₀	Input Keying Current	5		100	μA
I ₁₀	Input Switching Current		150		μA
I ₁₀	Input Blocking Current at V10-16 = -5V		<1		μA
Line Flyback Pulse					
I ₆	Input Current		>10		μA
V6-16	Input Switching Voltage		0.8		V
V6-16	Input Limiting Voltage	-0.7		1.4	V
R6-16	Input Resistance		0.4		kΩ
Pulse Duration Switch					
For t = 7 μs					
V4-16	Input Voltage	8.2		13.2	V
I ₄	Input Current		>200		μA
For t = 14 μs + t _d					
V4-16	Input Voltage	0		4.0	V
-I ₄	Input Current		>200		μA
For t = 0; V4-16 = 0					
V4-16	Input Voltage, (Note 1)		6.0		V
I ₄	Input Current (Input Open)		0		μA
Switching on VCR					
V11-16	Input Voltage, (Note 2)	0		1.5	V
V11-16	Input Voltage, (Note 2)	9		13.2	V
-I ₁₁	Input Current, (Note 2)		>200		μA
I ₁₁	Input Current, (Note 2)	1		2	mA
DELIVERED OUTPUT SIGNALS					
Vertical Sync Pulse (Positive-Going)					
V8-16 (p-p)	Output Voltage (Peak-to-Peak Value)	10	11		V
R8	Output Resistance		2		kΩ
Burst Gating Pulse (Positive-Going)					
V7-16	Output Voltage (Peak-to-Peak Value)	10	11		V
R7	Output Resistance		70		Ω

Electrical Characteristics (Continued)

PARAMETER		MIN	TYP	MAX	UNITS
DELIVERED OUTPUT SIGNALS (CONTINUED)					
Blanking Pulse					
V7-16 (p-p)	Output Voltage (Peak-to-Peak Value) TDA 2591		3.0		V
	TDA2593		4.5		V
R7	Output Resistance		70		Ω
Line Trigger Pulse (Positive-Going)					
V3-16 (p-p)	Output Voltage (Peak-to-Peak Value)		10.5		V
I3(AV)	Output Current (Average Value), (Note 3)		100		mA
R3-16	Output Resistance for Leading Edge of Line Pulse		2.5		Ω
R3-16	Output Resistance for Trailing Edge of Line Pulse		20		Ω
Oscillator					
V14-16	Threshold Voltage Low Level		4.4		V
V14-16	Threshold Voltage High Level		7.6		V
$\pm I_{14}$	Discharge Current		0.47		mA
V15-16	Current Source Supply Voltage		6.0		V
-I15	Current Source Supply Current		0.5		mA
Phase Comparison (ϕ_1; Sync Pulse-Oscillator)					
V13-16	Control Voltage Range	3.8		8.2	V
$\pm I_{13M}$	Control Current (Peak Value)	1.9	2.1	2.3	mA
I13	Output Blocking Current				μ A
	At V13-16 = 4-8V			1	
	Output Resistance				
	At V13-16 = 4-8V, High Ohmic (Note 4)				
	At V13-16 < 3.8V or > 8.2V, Low Ohmic, (Note 5)				
Time Constant Switch					
V12-16	Output Voltage		6		V
$\pm I_{12}$	Output Current			1	mA
	Output Resistance				
R12-16	At V11-16 = 2.5 to 7V		0.1		k Ω
R12-16	At V11-16 < 1.5V or > 9V		60		k Ω
Coincidence Detector (ϕ_3)					
V11-16	Output Voltage	0.5		6	V
	Output Current (Peak Value)				
I11M	Without Coincidence		0.1		mA
-I11M	With Coincidence		0.5		mA
Phase Comparison (ϕ_2; Oscillator-Line Flyback Pulse)					
V5-16	Control Voltage Range	5.4		7.6	V
$\pm I_5$	Control Current (Peak Value)		1		mA
	Output (Input) Resistance				
	At V5-16 = 5.4 to 7.6V, High Ohmic, (Note 4)				
R5-16	At V5-16 < 5.4V or > 7.6V		8		k Ω
I5	Input Current at Blocked Phase' Detector				μ A
	V5-16 = 6.5V			5	

Note 1: Can also be not connected.

Note 2: When supplied by the IC.

Note 3: Higher values are allowed when reducing P_{TOT} .

Note 4: Current source.

Note 5: Emitter follower.

Note 6: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Applications Information

PARAMETER		MIN	TYP	MAX	UNITS
Sync Separator					
V9-16 (p-p)	Input Voltage (Without Video; Peak-to-Peak Value)	1	3	7	V
I _g	Input Keying Control			100	μA
Noise Signal Keying					
V10-16 (p-p)	Input Voltage (Without Video; Peak-to-Peak Value)	1	3	7	V
I ₁₀	Input Keying Current			100	μA
V _{n(p-p)}	Superimposed Noise Voltage (Peak-to-Peak Value)			7	V
Vertical Sync Pulse Separator					
t _{ON}	Delay Between Leading Edge of Input and Output Signal		12		μs
t _{OFF}	Delay Between Trailing Edge of Input and Output Signal	t _{ON}			μs
V8-16 (p-p)	Output Voltage (Peak-to-Peak Value)	10	11		V
R8-16	Output Resistance		2		kΩ
Oscillator					
f _o	Frequency; Free Running (C14-16 = 4.7 nF, R15-16 = 12 kΩ)		15.625		kHz
Δf _o /f _o	Spread of Frequency, (Note 7)		<±5		%
Δf _o /ΔI ₁₅	Frequency Control Sensitivity		31		Hz/μA
Δf _o /f _o	Adjustment Range of Network in Figure 1		±10		%
$\frac{\Delta f_o/f_o}{\Delta V/V_{TYP}}$	Influence of Supply Voltage on Frequency at V1-16 = 12V, (Note 7)			5	%
Δf _o	Change of Frequency when V1-16 Drops to 4V			10	%
Phase Comparison (φ1; Sync Pulse-Oscillator)					
	Control Sensitivity		2		kHz/μs
	Spread of Control Sensitivity, (Note 7)		±10		%
Δf	Catching and Holding Range (82 kΩ)		±780		Hz
Δf/f	Spread of Catching and Holding Range, (Note 7)		±10		%
Phase Comparison (φ2; Oscillator-Line Flyback Pulse)					
t _d	Permissible Delay Between Leading Edge of Output Pulse and Leading Edge of Flyback Pulse			15	μs
Δt/Δt _d	Static Control Error		<0.2		%
Overall Phase Relation					
t	Phase Relation Between Middle of Sync Pulse and the Middle of the Flyback Pulse		2.6		μs
Δt	Tolerance of Phase Relation			0.7	μs
Adjustment Sensitivity, Caused By: (Note 8)					
ΔV5-16/Δt	Adjustment Voltage		0.1		V/μs
ΔI5/Δt	Adjustment Current		30		μA/μs
	Spread of Adjustment Current, (Note 7)		<10		%
Burst Gating Pulse					
t	Phase Relation Between Middle of Sync Pulse at the Input and the Leading Edge of the Burst Gating Pulse; V7-16 = 7V	2.15	2.65	3.15	μs
t7	Burst Gating Pulse Duration		4.0		μs

Applications Information (Continued)

PARAMETER		MIN	TYP	MAX	UNITS
t_p	Line Trigger Pulse				
	Output Pulse Duration				
t_p	At $V_4-16 > 8.2V$	5.5	7	8.5	μs
	At $V_4-16 < 4V$		$14 + t_d$		μs
V_1-16	Supply Voltage for Switching Off the Output Pulse	4			V
t_p	Internal Gating Pulse		7.5		μs
	Pulse Duration				

Note 7: Exclusive external components tolerances.

Note 8: The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase control ϕ_2 . The values beyond this point count if additional adjustment is required.

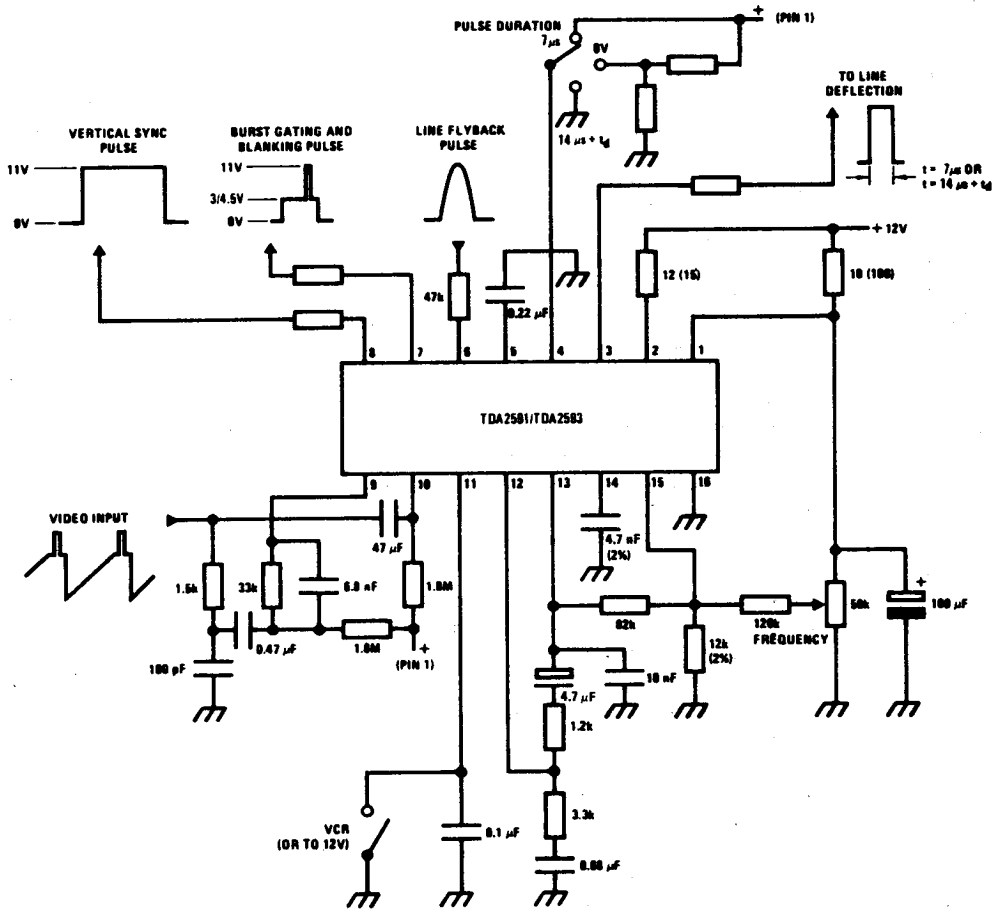
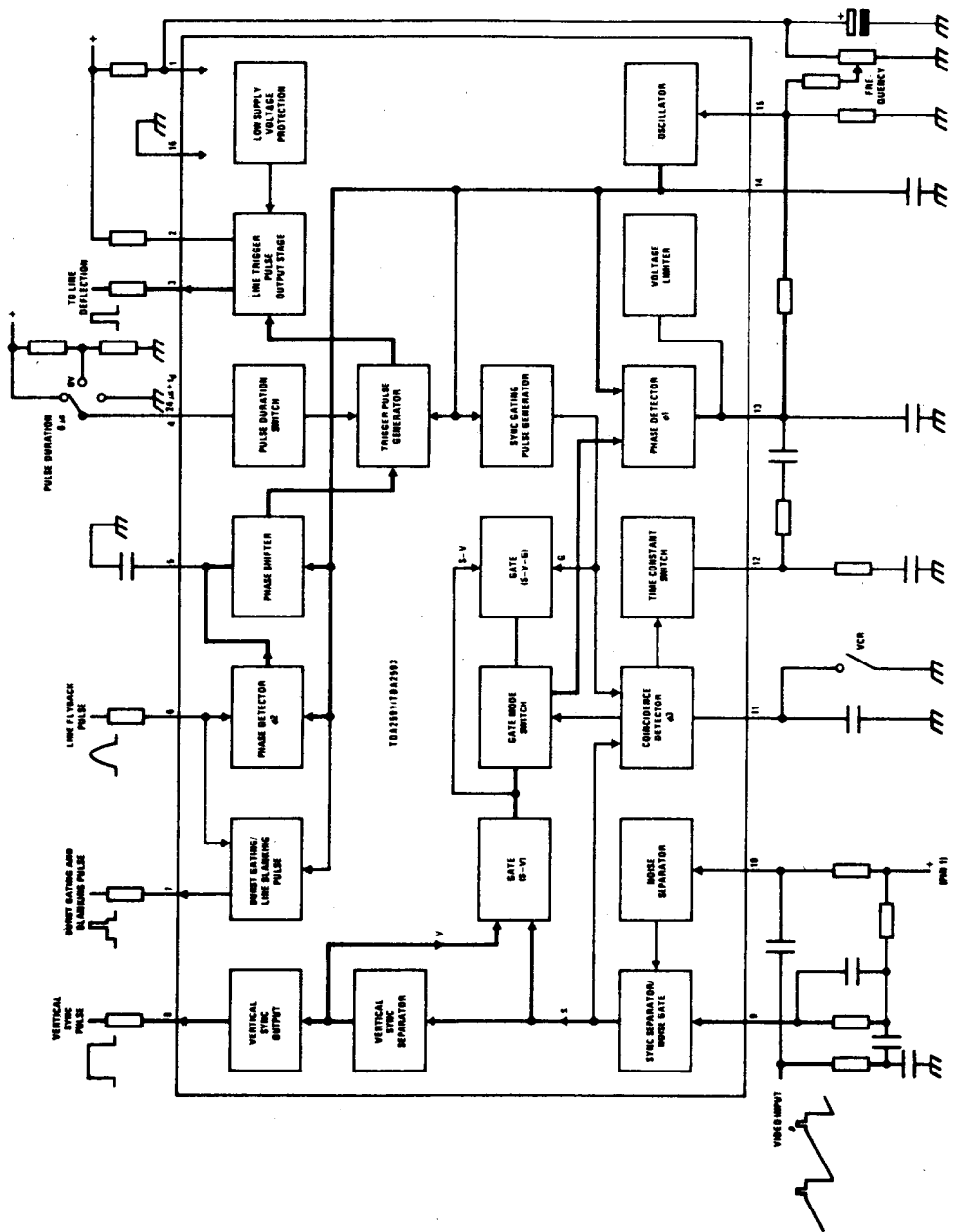


FIGURE 1

Block Diagram



TDA2591/TDA2593

