TMS 4006 JC, TMS 4006 NC
DIGITAL STORAGE BUFFER

features

- Asynchronous input and output clocks
- Serial or parallel input capability
- No minimum clock rate (long-term storage)
- Low output impedance
- Double-ended buffer
- 28-pin CDIP or dual-in-line plastic package
- Memory expansion by cascading units

description

The TMS 4006 JC/NC is a data storage register with a capacity of 11 or 13 words of 6 bits each. It performs storage on a first-in first-out basis. The device employs a method of storage commonly referred to as "silo" mode.

Input and output of the digital storage buffer operate entirely independently. A word is transferred into the TMS 4006 JC/NC on the positive-going edge of the data input clock (DIC). A word is transferred out of the register on the positive going edge of the data output clock (DOC).

The input and output clocks are completely independent of each other. There is no minimum clock rate. Logic used in the TMS 4006 JC/NC is purely static and the device has long-term retention.

Once a character is entered it will be stored temporarily in the first available register. A control logic associated with the next register will indicate whether or not that register already contains a valid word. If the next register is full, the input word will stay in the first register. If the next register is empty the word will fall down in parallel and be transferred. This operation will be repeated time after time until a full register is met. The operation is completely independent of the input, output clocks, and of all terminals.

The input word can be loaded either in serial or in parallel.

To load the device in parallel, the serial parallel (S/P) control must be at a logic 1.

To load in serial, the S/P control must be at a logical 0. A marker bit will be loaded concurrently with the first shift pulse (data input clock). This marker bit will be a logical 0. In serial mode the input word will then be 7 bits (1 marker bit and 6 data bits). Parallel inputs should be held at less than −10 volts or left floating. In parallel operation, the serial input should be held greater than −1.5 volts or left floating.

The TMS 4006 JC/NC can store 11 words when operating in the serial mode and 13 words when operating in the parallel mode.

When in serial mode a word cannot be "all zero"; at least one of the data bits must be a 1.

Several outputs will allow the user to find out how much data is stored in the TMS 4006 JC/NC:

A Flag 1 output will indicate whether the first (first-in word) register is full.

A Flag 10 output will indicate whether the 10th register is full.

A Flag 13 output will indicate whether the 13th register is full.

Flag outputs may be used to generate a readout command when a certain number of registers are full.

An ADIS (any data-in storage) output allows the user to detect lock-up, which may occur if power supplies are disconnected. Different outputs on ADIS and Flag 1 indicate lock-up. The register must then be cleared.

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description (continued)

A Clear input will allow the user to clear all the registers of the TMS 4006 JC/NC simultaneously.

TMS 4006 JC/NC can be connected in cascade or in parallel to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions, two controls are provided: a next-register input clock (NRC), which provides the input clock signal to the next register in a cascaded string, and a previous-register output clock (PRC) which provides the output clock signal to the previous register in a cascaded string.

"TMS 4006 JC" is the part number for a unit mounted in a 28-pin ceramic dual-in-line package. In a 28-pin plastic package the device is numbered "TMS 4006 NC".

operation

Transferring data into the device occurs on the positive-going edge of DIC. Output data appears on the positive-going edge of the DOC and resets to one on the negative-going edge of the DOC.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range* . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range* . . . . . −30 V to 0.3 V
Clock and data input voltage ranges* . . . . . −30 V to 0.5 V
Operating free-air temperature ranges . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

* These voltages are with respect to network ground terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNIT
Supply voltage V_{GG}	−23	−24	−28	V
Supply voltage V_{DD}	−13	−14	−18	V
Data input voltage				
$V_{in(0)}$ logical 0	0	−2.0	−3.0	V
$V_{in(1)}$ logical 1	−11	−12	−16	V
Clock input voltage				
$V_{\phi(0)}$ logical 0	0	−2.0	−3.0	V
$V_{\phi(1)}$ logical 1	−11	−12	−16	V
S/P input				
Serial mode	−0.3	0	−1.5	V
Parallel mode	−23	−24	−28	V
Clear command				
Logical 0	+0.3	0	−1.5	V
Logical 1	−23	−24	−28	V
Marker bit for serial input	0	−2.0	−3.0	V
Width of data pulse $t_{p(data)}$†	10			μsec
Rise-time of clock pulses, $t_{r(clock)}$†			2	μsec
Fall-time of clock pulses, $t_{f(clock)}$†			2	μsec
Clock repetition rate†	0		25.0	kHz
Width of clock pulses, $t_{p(clock)}$†	5			μsec
Overlap of data to clock, t_{OV}†	0	1.0		μsec

† See Timing Diagram

NOTE: Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies.

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electrical characteristics (under nominal operating conditions at 25°C unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage		−11		−16	V
$V_{out(0)}$	Logical 0 output voltage		−2.0	−2.5	−3.0	V
Z_{out}	Output impedance	V_{out} = 0 to 3 V		700	1000	Ω
	All flag outputs*	$R_L \leq$ 50 kΩ to GND	45			μA
PRC (1)	Previous register clock logical 1 level	$R_L \geq$500 kΩ to GND $C_L \leq$20 pF	−8	−10	−12	V
PRC (0)	Previous register clock logical 0 level	$R_L \geq$500 kΩ to GND, $C_L \leq$20 pF	−2.0	−2.5	−3.0	V
NRC (1)	Next register clock logical 1 level	$R_L \geq$500 kΩ to GND $C_L \leq$20 pF	−8	−10	−12	V
NRC (0)	Next register clock logical 0 level	$R_L \geq$500 kΩ to GND $C_L \leq$20 pF	−2.0	−2.5	−3.0	V
$I_{in(1)}$	Logical 1 level input leakage current	V_{in} = −15 V, V_{DD} = 0 V, V_{GG} = 0 V			6.0	μA
$I_{in(1)\phi}$	Logical 1 level input leakage current into the clock input	$V_{in\phi}$ = −20 V, V_{DD} = 0 V, V_{GG} = 0 V			10.0	μA
C_{in}	Capacitance of data input	V_{in} = 0 V, T_A = 25°C, $F_{(clock)}$ = 25 kHz		3.0	5.0	pF
$C_{in\phi}$	Capacitance of clock inputs	V_{in} = 0 V, T_A = 25°C, $F_{(clock)}$ = 25 kHz		3.0	5.0	pF
I_{DD}	Supply current into V_{DD} terminal	V_{DD} = −14 V, V_{GG} = −24 V		20	30	mA
I_{GG}	Supply current into V_{GG} terminal	V_{DD} = −14 V, V_{GG} = −24 V		4	10	mA
	Power dissipation			250		mW

* Includes SYNC, 1st Flag, 10th Flag, 13th Flag and ADIS.

switching characteristics

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from DIC to appearance of data at output of empty register (13 register levels of delay)	(See Timing Diagram)		5	7	μsec
t_{pd0}	Propagation delay time to logical 0 level from DIC to appearance of data at output of empty register (13 register levels of delay)	(See Timing Diagram)		5	7	μsec
t_{pda}	Propagation delay time to Flag 10 turn-on from DIC to appearance of data at level 10 (4 register levels of delay).	(See Timing Diagram)		1	2	μsec
t_{pdb}	Propagation delay time to Flag 10 turn-off from DOC to disappearance of data at level 10 (10 register levels of delay)	(See Timing Diagram)		3	5	μsec
t_{pdc}	Propagation delay time to Flag 13 turn-off from DOC to disappearance of data at level 13 (13 register levels of delay).	(See Timing Diagram)		5	7	μsec

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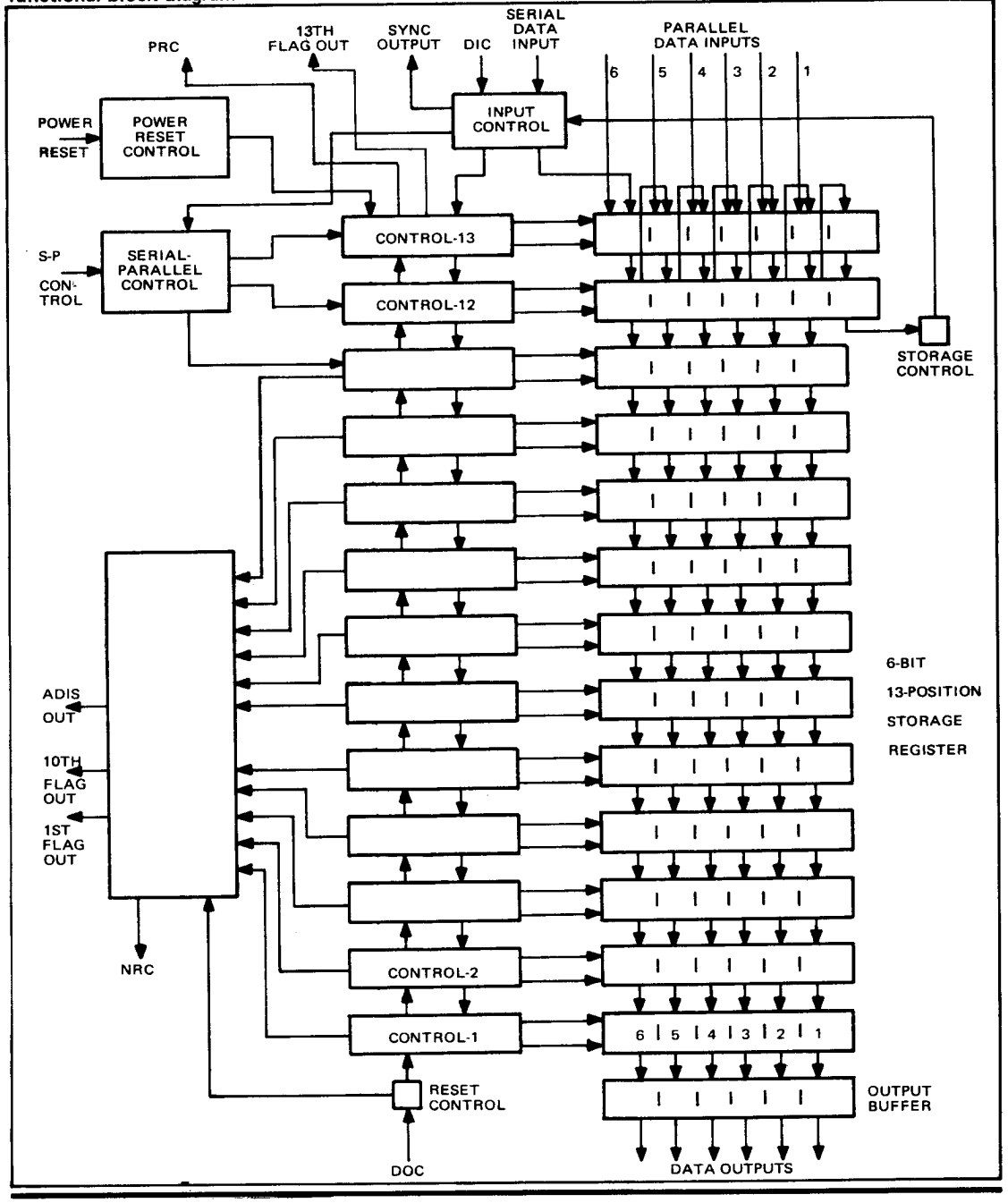
functional block diagram



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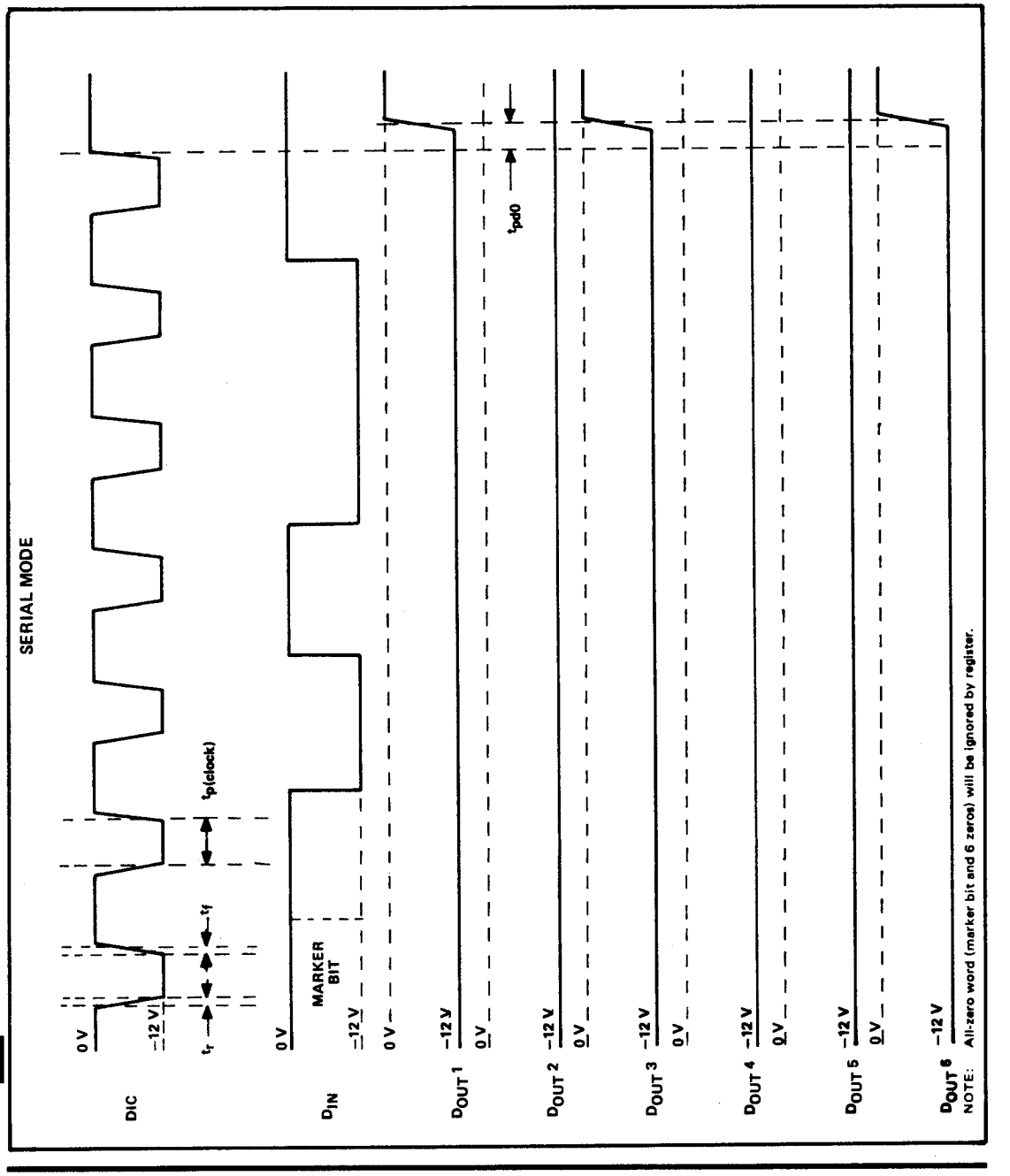
timing diagram and waveforms



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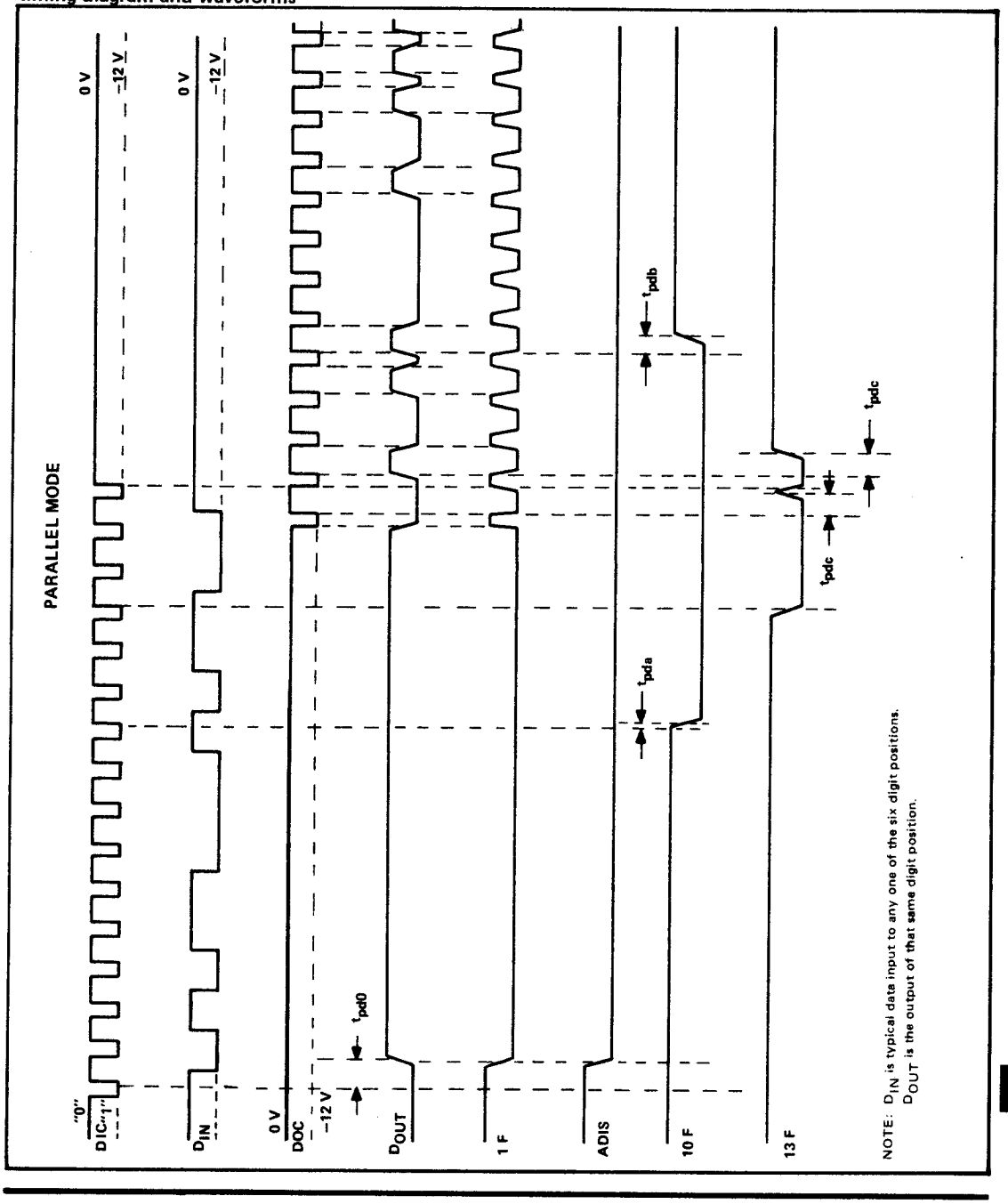
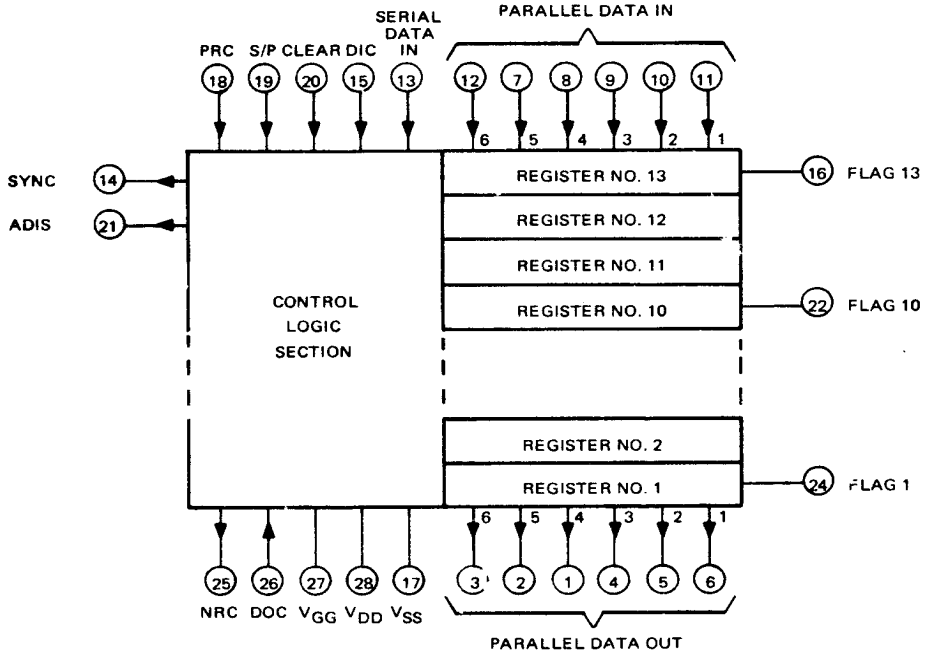
timing diagram and waveforms



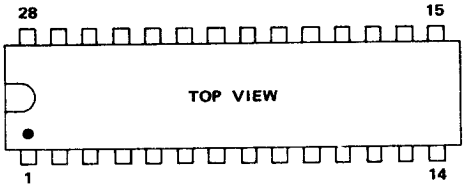
mechanical data

The digital storage buffer is available in both a 28-pin hermetically sealed dual-in-line package (TMS 4006 JC) and a 28-pin dual-in-line plastic package (TMS 4006 NC). The package is designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.).

pin configuration



PRC	–	PREVIOUS-REGISTER CLOCK
NRC	–	NEXT-REGISTER CLOCK
ADIS	–	ANY DATA IN STORAGE
S/P	–	SERIAL/PARALLEL CONTROL
DIC	–	DATA-INPUT CLOCK
DOC	–	DATA-OUTPUT CLOCK
V_{SS}	–	SUBSTRATE
V_{DD}	–	DRAIN POWER SUPPLY
V_{GG}	–	GATE POWER SUPPLY



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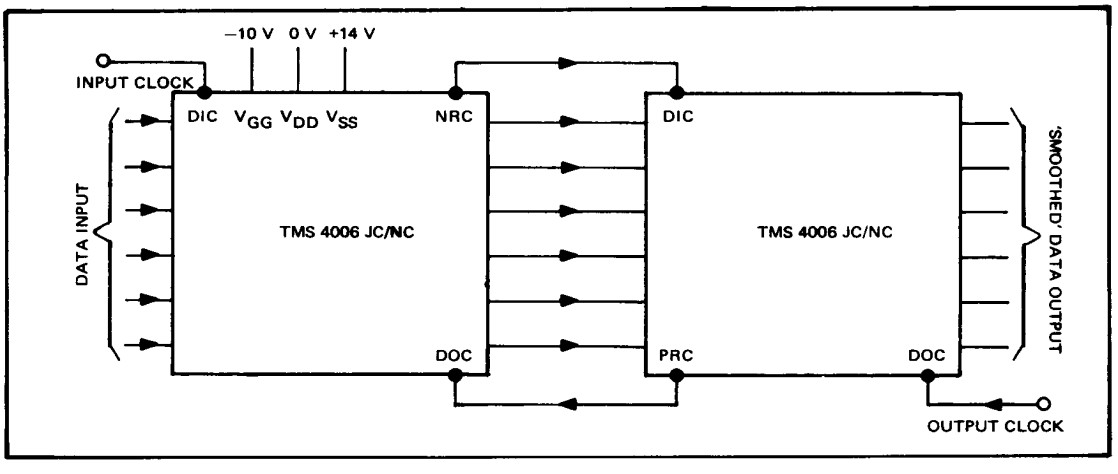
memory expansion

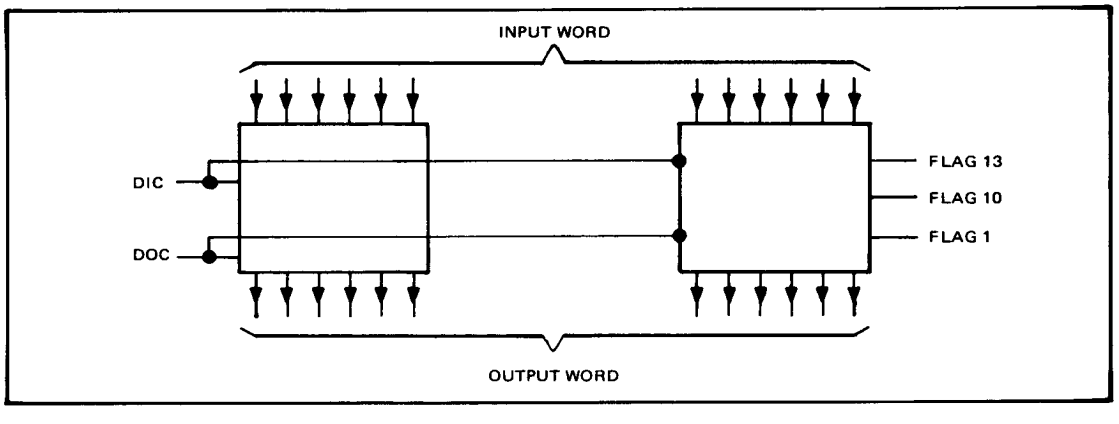
DSBs can be connected in cascade or in parallel to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions, two controls are provided: an NRC which provides the input clock signal to the next register in a cascaded string, and a PRC which provides the output clock signal to the previous register in a cascaded string. There is no limit, in terms of performance, to the number of registers in a cascaded string. To extend the digit positions, the input and output control signals of a number of registers are tied in parallel. N registers tied in this fashion to store 6N digit characters can only accept characters serially in 6-bit sub-characters with the restriction that a marker pulse must proceed each 6-bit sub-character. There are no restrictions on input character format in the parallel mode.

a) Cascading



Digital storage buffers can be cascaded very simply to provide extra capacity since all the control clocks and gating are generated internally permitting direct connection of one DSB to the next.

b) Paralleling



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