MOS
LSI

TMS 4020 NC
2048-BIT DYNAMIC RANDOM-ACCESS MEMORY

FEBRUARY 1971

features

- Low power dissipation
- Full decode
- Access time — 320 nsec max
- Cycle time — 640 nsec max
- High output-current capability (2 mA typ)
- Low-threshold technology
- 24-pin plastic package

description

The TMS 4020 NC is a 1024-word by 2-bit random-access memory, constructed on a single chip, with MOS P-channel enhancement-mode transistors. The device has two 1024-bit storage arrays with a 10-bit address decode common to both. There are four input chip selects — two for each array.

The address decode as well as the memory arrays are implemented with dynamic circuitry, thus enabling low power dissipation. Data stored in memory is nondestructively read. Refreshing of stored data is required every two milliseconds and refreshing the entire 2048 bits is accomplished with 16 Read cycles.

The outputs of the device are open ended, allowing several circuits to be wired-OR. The information read from the array is opposite in polarity to the write input.

The TMS 4020 NC is fabricated with a thick-oxide, low-threshold, self-aligned gate process.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

The Precharge Cycle ϕ_1 is used to set up the dynamic decode logic for address selection, which occurs during Generate Time ϕ_2.

During the Generate Time ϕ_2 the address decode is propagated and the memory arrays are precharged. With the return of ϕ_2 to the most positive voltage, the propagation of selected X-rows (1 of 16) of both arrays is initiated. The information in the two bits selected by the Y decode is then available at the output in 100 nsec.

If a Read cycle is required, the data can be sampled at this time. An additional 100 nsec is required in the cycle to assure the completion of the refresh cycle. If a Write cycle is required, the Write strobe should be initiated 130 nsec after the termination of the Generate ϕ_2 signal concurrent with the new information being written. The remaining positions in the X-row (not being written into) will complete the refresh cycle.

All X-rows not read during a 2-msec period should be refreshed via Read cycle to assure the integrity of the data.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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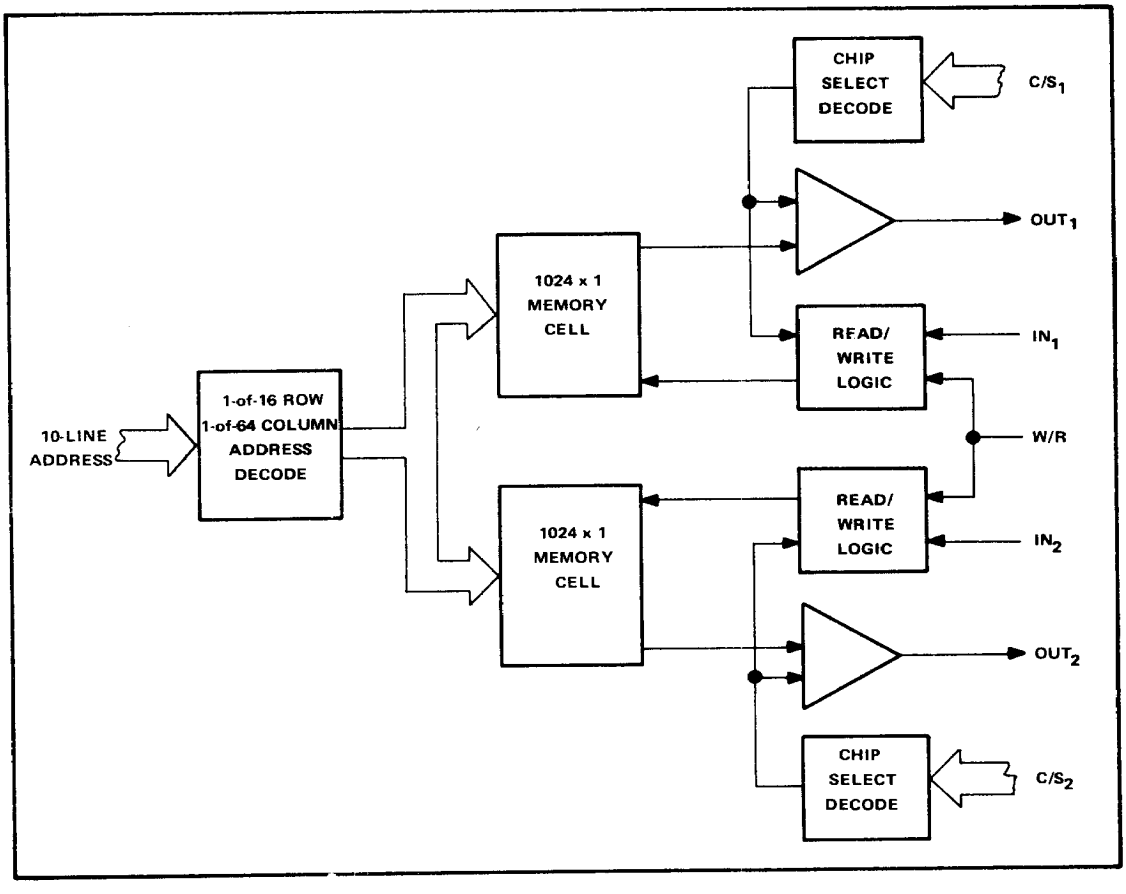
functional block diagram and pin configuration



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−25°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (substrate).

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recommended operating conditions (see note 2)

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate Voltage V_{SUB}	1.5	2.0	2.5	V
Drain supply V_{DD}	−17	−16	−15	V
Logic Levels				
Input HIGH level V_{IH}	−1.5	0	+0.3	V
Input LOW level V_{IL}	−17	−16	−15	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$	−1.0	0	+0.3	V
Clock LOW level $V_{\phi L}$	−17	−16	−15	V
Pulse Timing				
Pulse transition t_r, t_ϕ			1000	ns
Clock pulse width of ϕ_1 PW_1	90			ns
Clock pulse width ϕ_2 PW_2	170			ns
Clock delay from ϕ_1 to ϕ_2 P_{d1}	0			ns
Clock delay from ϕ_2 to ϕ_1 P_{d2} (Read and Refresh)	200			ns
Clock delay from ϕ_2 to ϕ_1 P_{d2} (Write)	310			ns
Address set-up time P_{AS}	0			ns
Address hold time P_{AH}	0			ns
ϕ_2-to-write pulse delay time P_{dW}	130			ns
Write pulse width P_{WW}	150			ns
Pulse Spacing				
Data set-up time P_{DS}	10			ns
Data hold time P_{DH}	10			ns
Chip select set-up time P_{CS}	0			ns
Chip select hold time P_{CH}	0			ns
Cycle time (Read and Refresh)	530			ns
Cycle time (Write)	640			ns
Strobe data width P_0	100			ns
Refreshing Time P_{REF}			2	ms

NOTE 2: These voltage values are with respect to V_{SS}.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Current $I_{OS(H)}$ Sense	Load = 100 Ω	1.2	2.0		mA
Output Leakage Current $I_{L(out)}$	V_{OUT} = −16 V			1	μA
Input (Load) Current $I_{L(in)}$	V_{IN} = −16 V			1	μA
Substrate Leakage Current I_{SUB}	V_{SUB} = +2 V			100	μA
Supply Current I_{DD}					
During PW_1			15	20	mA
During PW_2			26	34	mA
During P_{d2}			1.5	2	mA
Average Supply Current $I_{DD(AV)}$			13	18	mA

14

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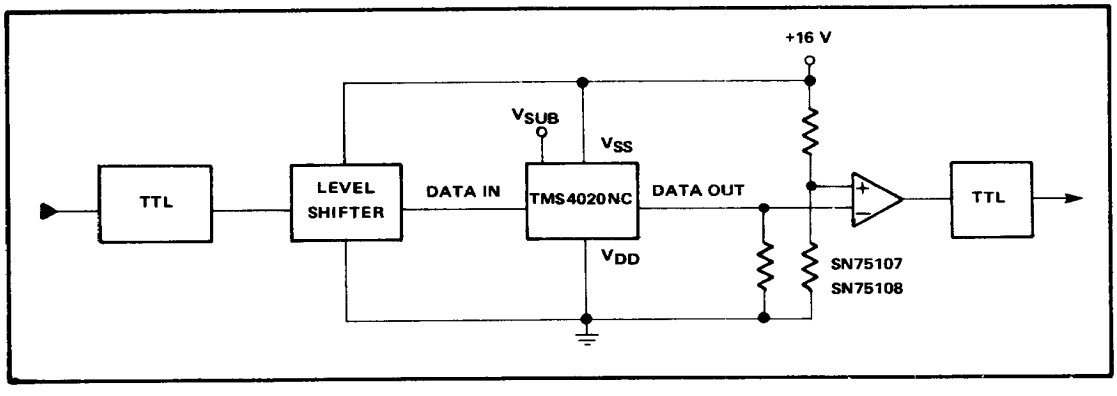
dynamic electrical characteristics (under nominal operating conditions from 0°C to +70°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
End of ϕ_2 to output delay P_{d0}	LOAD = 100 Ω		70	100	ns
Address to output access time P_{ACC1}	$I_{OS(HIGH)}$ = 0.8 mA min		290	320	ns
ϕ_1 to output access time P_{ACC2}	$I_{OS(LOW)}$ = 0.2 mA min		410	440	ns
Address Capacitance					
A_0 through A_3	F = 1 MHz at 25°C,		8	11	pF
A_4 through A_8	$V_{AF} = V_{SS}$		6	8	pF
A_9			4	6	pF
Clock Capacitance					
ϕ_1	F = 1 MHz,		18	22	pF
ϕ_2	$V_\phi = V_{SS}$ at 25°C		30	38	pF
Read/Write Capacitance					
Chips selected	F = 1 MHz,		27	33	pF
Chips not selected	$V_{R/W} = V_{SS}$ at 25°C		15	20	pF
Data Input Capacitance					
Chips selected	F = 1 MHz,		20	25	pF
Chips not selected	$V_{in} = V_{SS}$ at 25°C		5	7	pF
Data Output Capacitance					
Chips selected	F = 1 MHz,		8	12	pF
Chips not selected	$V_{out} = V_{SS}$ at 25°C		3	5	pF

TTL interface



14

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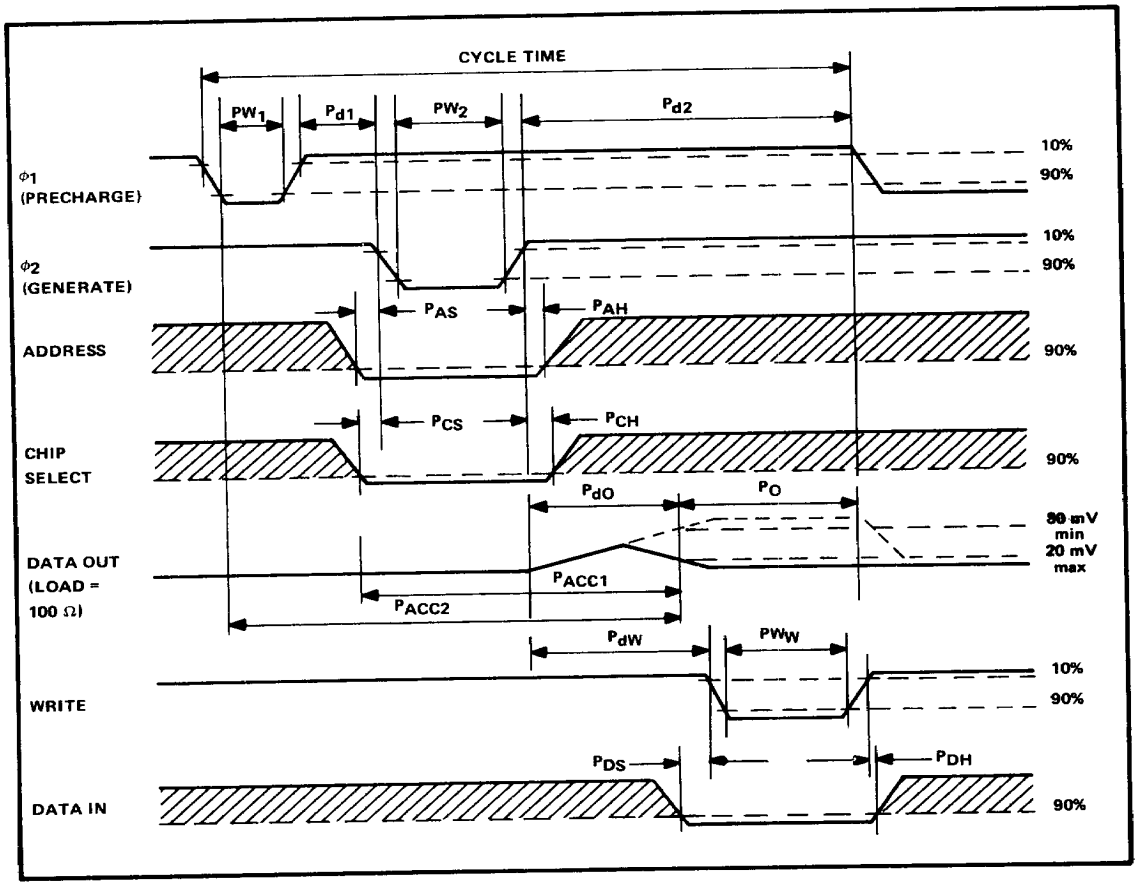
timing diagram and voltage waveforms



14

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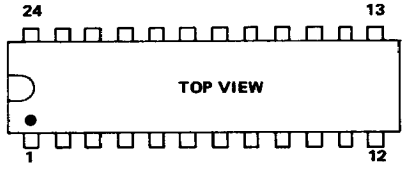
mechanical data

The TMS 4020 NC is mounted in a 24-pin plastic dual-in-line package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_6	13	A_1
2	A_5	14	A_0
3	A_4	15	ϕ_2
4	$\overline{IN_1}$	16	C/S_2
5	OUT_1	17	C/S_2
6	C/S_1	18	R/W
7	C/S_1	19	OUT_2
8	ϕ_1	20	$\overline{IN_2}$
9	A_3	21	A_9
10	A_2	22	A_8
11	V_{SUB}	23	A_7
12	V_{DD}	24	V_{SS}

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