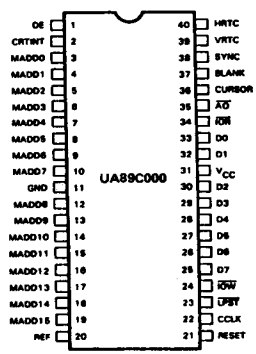
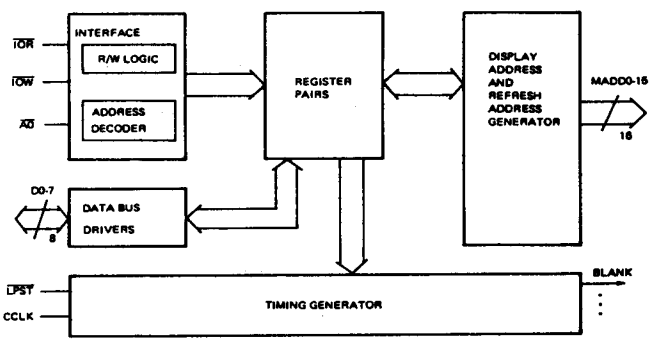
General Description

The UA89C000 CRT Controller contains 27 internal control registers to generate horizontal and vertical synchronous timings, addressing for the regenerative buffer, cursor and underline timings, and refresh addressing for DRAMs.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Type	Symbol	Description
1	O	DE	Display Enable is an active high output. It enables the display area on the screen. When DE and Blank signals are inactive at the same time, the border is displayed on the monitor.
2	O	CRTINT	CRT Interrupt is an active high output. It is enabled by bit 5 of the Vertical Retrace End register. It can be cleared by programming bit 4 of the Vertical Retrace End register to 0.
3	O	MADD 0	Memory Addresses are used to access the display memory.
4	O	MADD 1	
5	O	MADD 2	
6	O	MADD 3	
7	O	MADD 4	
8	O	MADD 5	

Pin Description (continued)

Pin No.	Type	Symbol	Description
9 10	O O	MADD 6 MADD 7	Memory Addresses are used to access the display memory.
11		GND	Ground
12 13 14 15 16 17 18 19	O O O O O O O O	MADD 8 MADD 9 MADD 10 MADD 11 MADD 12 MADD 13 MADD 14 MADD 15	Memory Addresses are used to access the display memory.
20	0	REF	Refresh is an active high output. It enables MADD(0-7) to refresh addressing.
21	I	RESET	RESET initializes the CRT Controller.
22	I	CCLK	The character clock comes from the sequencer and is used to synchronize all the functions for the device except the bus interface.
23	I	$\overline{\text{LPST}}$	A low-to-high transition of the $\overline{\text{LPST}}$ line latches the current refresh address in the internal light pen register.
24	I	$\overline{\text{IOW}}$	A low-to-high transition of the $\overline{\text{IOW}}$ line strobes the DB(7:0) bus to the CRTC's internal register during I/O write operation.
25 26 27 28 29 30	I/O I/O I/O I/O I/O I/O	D7 D6 D5 D4 D3 D2	The DB(7:0) lines connect the CRTC's 8-bit interface to an external microprocessor data bus. During register write operations, this is the input data bus. During register read operations, this is the output data bus.
31		V_{CC}	+5V power supply.
32 33	I/O I/O	D1 D0	Same as D7.
34	I	$\overline{\text{IOR}}$	A low-to-high transition of the $\overline{\text{IOR}}$ line strobes the data of the CRTC's internal register to the DB(7:0) bus during I/O read operation.
35	I	$\overline{\text{A0}}$	The $\overline{\text{A0}}$ input line is used to address the CRTC's internal register.
36	I	CURSOR	This indicates a valid cursor postion when DE is active. During the trailing edge of Blank signal, it signifies the contents of the Underline Location.
37	I	BLANK	When the BLANK line is high, the display is in blanking mode.
38	I	SYNC	A high-active SYNC line indicates a time slot allocation for R/W display memory operations to be performed by the CPU.
39	I	VRTC	Vertical retrace synchronization signal.
40	I	HRTC	Horizontal retrace synchronization signal.