

Description

The μPD72022 Intelligent Display Processor (IDP) performs CRT display control and image display data processing for text, static pictures, and sprites.

Features

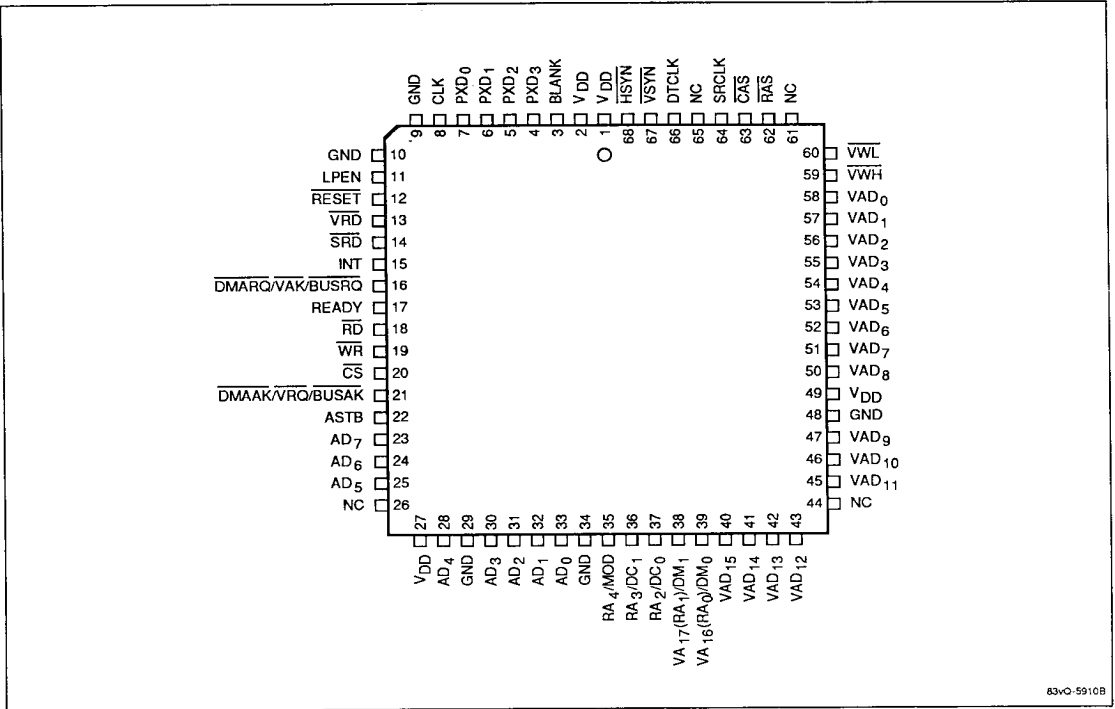
- Three display modes: text, semigraphics, graphics
- Four-way horizontal split-screen display
- Smooth-scroll control (vertical, horizontal)
- Sprite image display
- 16-color display
- Attribute addition (7 max)
- Interlaced display through external synchronization
- Up to 256K x 16-bit word video memory addressing
- DRAM refresh
- Optional dual-port RAM
- Bus arbitration control
- CRT control signal programmable variables
 - Horizontal display time, retrace time (left and right), sync pulse width
 - Vertical display time, retrace time, sync pulse width
 - Rasters/line
 - Blinking time
- Variable display resolution
 - Horizontal: 640 dots max (22-MHz max dot rate)
 - Vertical: 512 dots max
 - Display signal (4 bits/dot) serial output
- Horizontal and vertical external synchronization
- 22 screen-control/drawing commands
- CMOS
- Single +5-volt power supply

Ordering Information

Part Number	Package
μPD72022GF-3B9	80-pin plastic miniflat
μPD72022L	68-pin PLCC

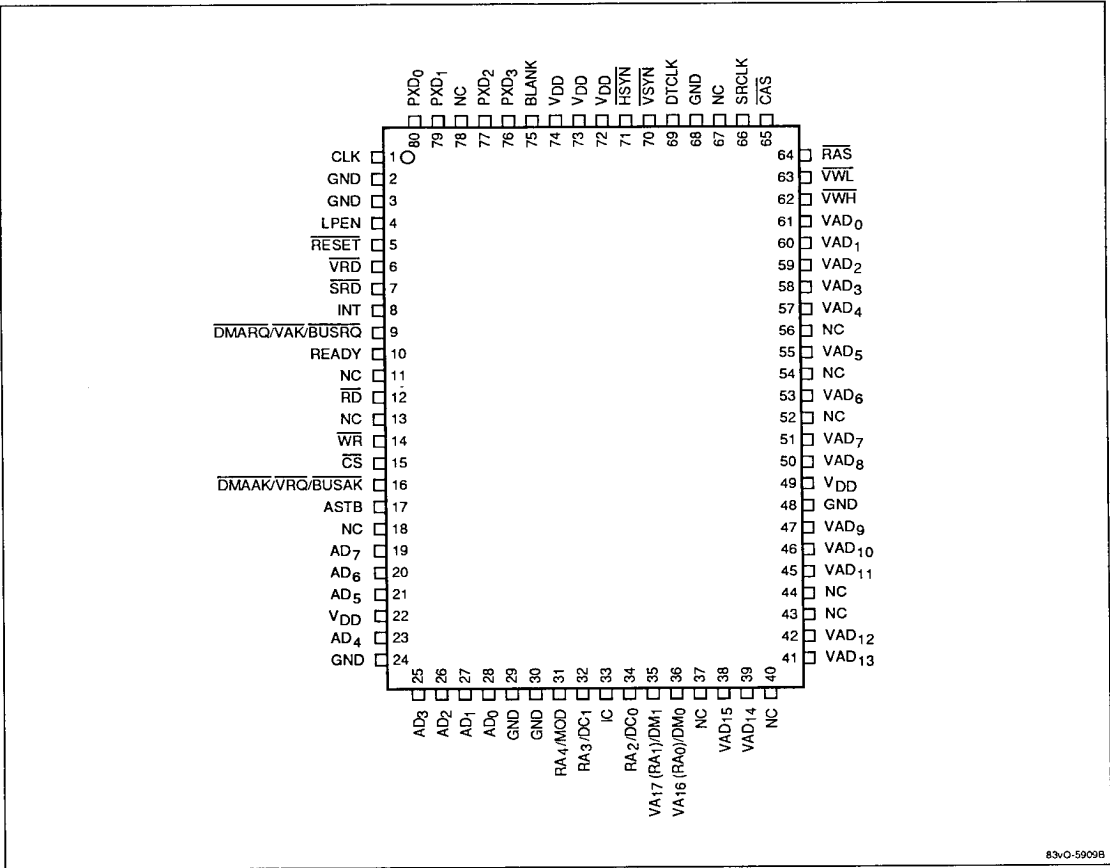
Pin Configurations

68-Pin PLCC



83V-C-5910B

80-Pin Plastic Miniflat



83vO-5909B

3

Pin Identification

Symbol	I/O	Signal Function
Host System Interface		
AD ₀ -AD ₇	I/O	Three-state, bidirectional address/data bus. See table 1.
ASTB	In	Address Strobe. Read address information from AD ₀ -AD ₇ .
BUSAK	In	Bus Acknowledge. While this signal is active, μPD72022 controls the system bus.
BUSRQ	Out	Bus Request. Request for system bus control.
CLK	In	System clock.
CS	In	Chip Select. Enables RD and WR signals.
DMAAK	In	DMA Acknowledge. Enables DMA cycle.
DMARQ	Out	DMA Request.
INT	Out	Interrupt request to host processor.
RD	In	Control signal for reading data or status flag from μPD72022.
READY	Out	Indicates μPD72022 may be accessed for memory read/write cycle or I/O read/write cycle.
RESET	In	Initializes μPD72022.
VAK	Out	Video Memory Acknowledge. Indicates host processor has direct control of video memory.
VRQ	In	Video Memory Request. Host processor requests direct control of video memory.
WR	In	Control signal for writing data, commands, or parameters into μPD72022.

Video Memory Interface

CAS	Out	Column Address Strobe.
MOD	In	Mode change signal. See RA ₄ .
RA ₀ -RA ₁	Out	Raster Address 0-1. RA ₀ and RA ₁ are also used for DM ₀ and DM ₁ , respectively. See Display Data Control in this table.
RA ₂ -RA ₃	Out	Raster Address 2-3. RA ₂ and RA ₃ are also used for DC ₀ and DC ₁ , respectively. See Display Data Control in this table.
RA ₄	Out	Raster Address 4. RA ₄ is also used for MOD input.
RAS	Out	Row Address Strobe.
SRCLK	Out	Serial Read Clock. Used with optional dual-port RAM.
SRD	Out	Serial Read. Active while data is read from serial port with optional dual-port RAM.
VAD ₀ -VAD ₁₅	I/O	Video Memory Address 0-15 output; DRAM refresh address output; data input/output.
VA ₁₆ -VA ₁₇	Out	Video Memory Address 16-17. Also used for RA ₀ , RA ₁

Symbol	I/O	Signal Function
VRD	Out	Video Memory Read. Strobe signal to read data from video memory.
VWH, VWL	Out	Video Memory Write, High and Low. Strobe signals to write data into video memory.

CRT Interface

BLANK	Out	Blanking display signal.						
DTCLK	I/O	Dot Clock. During internal DTCLK mode, timing pulses derived by dividing CLK are output. During external DTCLK mode, the internal scanning subsystem derives a reference clock from the DTCLK input.						
HSYN	I/O	Horizontal Sync. Signal output when internal sync is specified; signal input when external sync is specified.						
LPEN	In	Light Pen Strobe. The DTCLK mode is specified by the LPEN level when the RESET signal level rises. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>LPEN</th> <th>DTCLK Mode</th> </tr> </thead> <tbody> <tr> <td>High</td> <td>Internal DTCLK output</td> </tr> <tr> <td>Low</td> <td>External DTCLK input</td> </tr> </tbody> </table>	LPEN	DTCLK Mode	High	Internal DTCLK output	Low	External DTCLK input
LPEN	DTCLK Mode							
High	Internal DTCLK output							
Low	External DTCLK input							
PXD ₀ -PXD ₃	Out	Pixel Data 0-3. Display signal (four bits/dot) in sync with DTCLK.						
VSYN	I/O	Vertical Sync. Signal output when internal sync is specified; signal input when external sync is specified.						

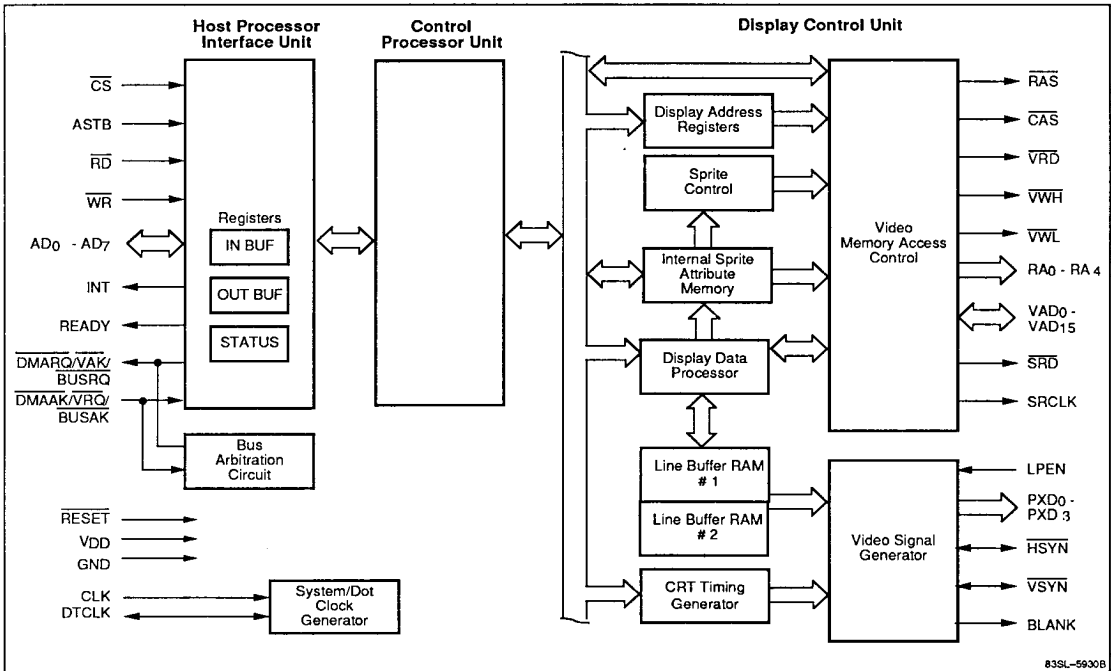
Display Data Control

DC ₀ , DC ₁	Out	Display Cycle. Specifies display processing cycle when μPD72022 is accessing video memory. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DC₁</th> <th>DC₀</th> <th>Display Cycle</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Other than indicated below</td> </tr> <tr> <td>0</td> <td>1</td> <td>Static picture display cycle</td> </tr> <tr> <td>1</td> <td>0</td> <td>Sprite display cycle</td> </tr> <tr> <td>1</td> <td>1</td> <td>Screen start cycle</td> </tr> </tbody> </table> See Video Memory Interface, RA ₂ and RA ₃ .	DC ₁	DC ₀	Display Cycle	0	0	Other than indicated below	0	1	Static picture display cycle	1	0	Sprite display cycle	1	1	Screen start cycle
DC ₁	DC ₀	Display Cycle															
0	0	Other than indicated below															
0	1	Static picture display cycle															
1	0	Sprite display cycle															
1	1	Screen start cycle															
DM ₀ , DM ₁	Out	Display Mode. Specifies the static picture display mode. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DM₁</th> <th>DM₀</th> <th>Display Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>x</td> <td>Text mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>Semigraphics mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>Graphics mode</td> </tr> </tbody> </table> See Video Memory Interface, RA ₀ and RA ₁ .	DM ₁	DM ₀	Display Mode	0	x	Text mode	1	0	Semigraphics mode	1	1	Graphics mode			
DM ₁	DM ₀	Display Mode															
0	x	Text mode															
1	0	Semigraphics mode															
1	1	Graphics mode															

Other Pins

GND	Ground
VDD	+5-volt power supply
NC	No Connection

μPD72022 Block Diagram



83SL-5930B

3

Table 1. Functions of Address/Data Bus AD₀-AD₇

CS	DMAAK	WR	RD	AD ₂	AD ₁	AD ₀	Bus Function
1	1	x	x	x	x	x	Floating (high impedance)
0	1	0	1	0	1	0	μPD72022 command input
				1	1	1	
				0	1	1	μPD72022 parameter input
				1	1	0	
1	0	0	1	x	x	x	Write operation via DMA transfer
0	1	1	0	0	1	0	μPD72022 status output
				1	1	1	
				0	1	1	μPD72022 parameter output
				1	1	0	
1	0	1	0	x	x	x	Read operation via DMA transfer

x = Don't care

Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V _{DD}	-0.5 to +7.0 V
Input voltage, V _I	-0.5 to +7.0 V
Output voltage, V _O	-0.5 to +7.0 V
Operating temperature, T _{OPT}	-10 to +70°C
Storage temperature, T _{STG}	-65 to +150°C

Capacitance

T_A = +25°C; V_{DD} = GND = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Input capacitance	C _I	10		pF	Unmeasured pins returned to 0 V
Output capacitance	C _O	20		pF	
Input/output capacitance	C _{IO}	20		pF	
Clock input capacitance	C _C	20		pF	

AC Characteristics

T_A = -10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
Clock						
System clock cycle	2	t _{CY}	45	50	ns	
System clock width, high	2	t _{KKH}	18		ns	
System clock width, low	2	t _{KKL}	18		ns	
Dot clock cycle	2	t _{CYDK}	45	4 t _{CY}	ns	Input; C _L = 30 pF
			67.5	4 t _{CY}	ns	Output; C _L = 30 pF
Dot clock width, high	2	t _{DKDH}	18		ns	Input; C _L = 30 pF
			t _{KKH}		ns	Output; C _L = 30 pF
Dot clock width, low	2	t _{DKDL}	18		ns	
Reset						
RESET pulse width	3	t _{RSRSL}	8 t _{CY} + 6 t _{CYDK}		ns	
LPEN setup time to RESET ↑	3	t _{SLPRS}	16 t _{CY}			
LPEN hold time from RESET ↑	3	t _{HRSLP}	0			
CPU Read/Write Cycle						
ASTB pulse width	4, 5	t _{STSTH}	45		ns	
Address setup time to ASTB ↓	4, 5	t _{SAST}	25		ns	
Address hold time from ASTB ↓	4, 5	t _{HAST}	10		ns	
C _S setup time to RD or WR ↓	4, 5	t _{SCSRW}	0		ns	

DC Characteristics

T_A = -10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Max	Unit	Conditions
Input low voltage	V _{IL}	-0.5	0.8	V	Note 1
		-0.5	0.6	V	Note 2
Input high voltage	V _{IH}	2.2	V _{DD} + 0.5	V	Note 1
		3.5	V _{DD} + 1.0	V	Note 2
Output low voltage	V _{OL}		0.45	V	I _{OL} = 2.2 mA
Output high voltage	V _{OH}	0.7 V _{DD}		V	I _{OH} = -400 μA
Input low leakage current	I _{LIL}		-10	μA	V _I = 0 V
Input high leakage current	I _{LIH}		10	μA	V _I = V _{DD}
Output low leakage current	I _{LOL}		-10	μA	V _I = 0 V
Output high leakage current	I _{LOH}		10	μA	V _I = V _{DD}
Power supply current	I _{DD}		150	mA	

Notes:

- (1) Except CLK, DTCLK, and $\overline{\text{RESET}}$
- (2) CLK, DTCLK, and $\overline{\text{RESET}}$

AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
CPU Read/Write Cycle (cont)						
CS hold time from \overline{RD} or \overline{WR} ↑	4, 5	t_{HRWCS}	0		ns	
\overline{RD} pulse width	4, 15	t_{RRL}	170		ns	
Data delay time from \overline{RD} ↓	4, 15	t_{DRD}	120		ns	
Data hold time from \overline{RD} ↑	4, 15	t_{HRD}	0		ns	
Data float time from \overline{RD} ↑	4, 15	t_{FRD}		55	ns	
\overline{WR} pulse width	5, 16	t_{WWL}	180		ns	
Data setup time to \overline{WR} ↑	5, 16	t_{SDW}	100		ns	
Data hold time from \overline{WR} ↑	5, 16	t_{HWD}	10		ns	
READY delay time from \overline{RD} or \overline{WR} ↓	4, 5, 16	t_{DRWRDY}		55	ns	
READY delay time from \overline{VRQ} ↓	9	t_{DVQRDY}		60	ns	
\overline{RD} recovery time	4	t_{RVR}	150		ns	
\overline{WR} recovery time	5	t_{RWV}	150		ns	
Read access cycle	4	t_{CYR}	$t_{RRL} + 10 t_{CY}$		ns	
Write access cycle	5	t_{CYW}	$t_{WWL} + 10 t_{CY}$		ns	
VRAM Read/Write Cycle						
Random read/write cycle	6-8, 11-13	t_{CYRAS}	270		ns	Note 1; also refresh cycle
			360		ns	Note 2; also data transfer cycle
\overline{RAS} width high	6-8, 11-13	$t_{RASRASH}$	95		ns	
\overline{RAS} width low	6-8, 11-13	$t_{RASRASL}$	130		ns	Note 1; also refresh cycle
			210		ns	Note 2; also data transfer cycle
\overline{CAS} width high	6-7, 11-13	$t_{CASCASH}$	110		ns	
\overline{CAS} width low	6-7, 11-13	$t_{CASCASL}$	105		ns	Note 1
			185		ns	Note 2; also data transfer cycle
\overline{RAS} ↓ delay time from \overline{CAS} ↑	6-8, 11-13	$t_{DCASRASL}$	30		ns	
\overline{CAS} ↓ delay time from \overline{RAS} ↓	6-7, 11-13	$t_{DRASCASL}$	40		ns	
\overline{RAS} ↑ delay time from \overline{CAS} ↓	6-7, 11-13	$t_{DCASRASH}$	60		ns	Note 1
			150		ns	Note 2; also data transfer cycle
Address setup time to \overline{RAS} ↓	6-8, 11-13	t_{SVARAS}	35		ns	
Address hold time from \overline{RAS} ↓	6-8, 11-13	t_{HRASVA}	10		ns	
Mode setup time to \overline{CAS} ↓	6-7, 11-13	t_{SMDCAS}	10		ns	
Mode hold time from \overline{CAS} ↓	6-7, 11-13	t_{HCASMD}	110		ns	Note 1
			185		ns	Note 2

AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
VRAM Read/Write Cycle (cont)						
VRD ↑ delay time from CAS ↓	6, 12-13	t _{DCASVR}	70		ns	Note 1
			150		ns	Note 2
CAS ↑ delay time from VRD ↑	6, 11-13	t _{DVRCAS}	0		ns	
VRD pulse width	6, 12-13	t _{VRRL}	70		ns	Note 1
			150		ns	Note 2
CAS ↓ delay time from VW ↑	6	t _{DVWHCAS}	70		ns	
VW ↓ delay time from RAS ↑	6	t _{DRASHWW}	35		ns	
VW ↓ delay time from CAS ↑	6	t _{DCASWL}	15		ns	
Input data setup time to VRD ↑	6	t _{SDVR}	40		ns	
Input data hold time from VRD ↑	6	t _{HVRD}	0	30	ns	
VRD ↑ delay time from RAS ↓	6, 12-13	t _{DRASVRH}	130		ns	Note 1
			210		ns	Note 2
RAS ↓ setup time from VRD ↑	6, 12-13	t _{SVRRAS}	15		ns	
VRD ↓ hold time from RAS ↓	6, 12-13	t _{HRASVR}	25		ns	
VRAM Write Cycle						
RAS ↓ delay time from VRD ↑	7	t _{DVRRAS}	15		ns	
VRD ↓ delay time from RAS ↓	7	t _{DRASVRL}	130		ns	
RAS ↓ delay time from VW ↑	7	t _{DVWRAS}	35		ns	
VW ↑ delay time from RAS ↓	7	t _{DRASLW}	-10		ns	
CAS ↓ delay time from VW ↓	7	t _{DVWLCAS}	10		ns	
VW ↑ delay time from CAS ↓	7	t _{DCASVWH}	155		ns	
VW pulse width	7	t _{VWWWL}	165		ns	
Data setup time to CAS ↓	7	t _{SDCAS}	10		ns	
Data hold time from CAS ↓	7	t _{HCASD}	155		ns	
VRAM Refresh Cycle						
CAS ↓ delay time from RAS ↑	8	t _{DRASHCAS}	20		ns	
VRAM Request						
VAK setup time to CAS ↑	9	t _{SVACAS}	20		ns	Interleave mode
VAK hold time from CAS ↓	9	t _{HCASVA}	10		ns	
VRQ recovery time	9	t _{FRVQ}	10 t _{CY}		ns	
READY delay time from VRQ ↓	9	t _{DVQRDY}		60	ns	
VRQ hold time from READY ↑	9	t _{HRDYVQ}	0		ns	
VAD float delay time from CAS ↑	9, 10	t _{FCASVAD}		30	ns	
VAD delay time from CAS ↑	9, 10	t _{DCASVAD}		50	ns	

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AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
VRAM Request (cont)						
BURSQ ↓ delay time from BUSAK ↑	10	t _{DBABQ}	0		ns	Dual-port mode
BUSAK hold time from BUSRQ ↑	10	t _{HBQHBA}	10		ns	
BUSAK hold time from BUSRQ ↓	10	t _{HBQLBA}	0	2000	ns	
Data Transfer Cycle						
VRD ↑ delay time from SRCLK ↑	11	t _{DSKVR}	100		ns	
SRCLK hold time from VRD ↑	11	t _{HVRSK}	100		ns	
RAS ↓ delay time from VRD ↓	11	t _{DVRRASL}	30		ns	
VRD hold time from RAS ↓	11	t _{HRASLVR}	60		ns	
VRD hold time from CAS ↓	11	t _{HCASVR}	10		ns	
RAS ↑ delay time from VRD ↓	11	t _{DVRRASH}	100		ns	
CAS ↑ delay time from VRD ↑	11	t _{DVRCAS}	120		ns	
VRD hold time from RAS ↑	11	t _{HRASHVR}	10		ns	
VRAM Serial Read Cycle						
SRD width high	12, 13	t _{SRSRH}	200		ns	
SRD width low	12, 13	t _{SRSRL}	200		ns	
SRCLK ↓ delay time from SRD ↓	12, 13	t _{DSRSK}	15		ns	
SRCLK width high	12, 13	t _{SKSKH}	25		ns	
SRCLK width low	12, 13	t _{SKSKL}	25		ns	
Serial read cycle	12, 13	t _{CYSK}	90		ns	
Data setup time to SRCLK ↑	12	t _{SDSK}	25		ns	Graphics display cycle
Data hold time from SRCLK ↑	12	t _{HSKD}	10		ns	
Data setup time to VRD ↑	13	t _{SDVR}	40		ns	Text display cycle
Data hold time from VRD ↑	13	t _{HVRD}	0	30	ns	Semigraphics display cycle
Display Timing						
Output display time from DTCLK ↑	14	t _{DDKDSP}	5	38	ns	Note 3; C _L = 50 pF
Input setup time to DTCLK ↑	14	t _{SDIK}	25		ns	Note 4
Input hold time from DTCLK ↑	14	t _{HDKI}	5		ns	
Input pulse width	14	t _i	6 t _{CYDK}		ns	
DMA Cycle						
DMAHQ ↑ delay time from DMAAK ↓	15, 16	t _{DDADQH}		50	ns	
DMAHQ ↓ delay time from DMAAK ↑	15, 16	t _{DDADQL}	0		ns	
DMAAK hold time to DMARK ↓	15, 16	t _{HQDA}	0		ns	
DMAAK setup time to RD ↓	15	t _{SDAR}	0		ns	
DMAAK hold time to RD ↑	15	t _{HRDA}	20		ns	
DMAAK setup time to WR ↓	16	t _{SDAW}	0		ns	
DMAAK hold time to WR ↑	16	t _{HWDA}	20		ns	

AC Characteristics (cont)

Parameter	Figure	Symbol	Min	Max	Unit	Conditions
Interrupt						
INT rising time	17	t_{INTR}		30	ns	
INT falling time	17	t_{INTF}		30	ns	

Notes:

- (1) Cycles: Text display; Semigraphics display; Display start
- (2) Cycles: Graphics display; Sprite display; Command processing
- (3) HSYN, VSYN, BLANK, PXD0-PXD3
- (4) HSYN, VSYN, LPEN

Figure 1. Voltage Thresholds for Timing Measurements

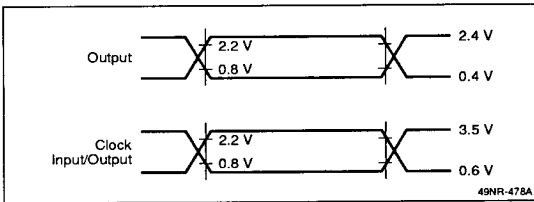


Figure 3. Reset Waveform

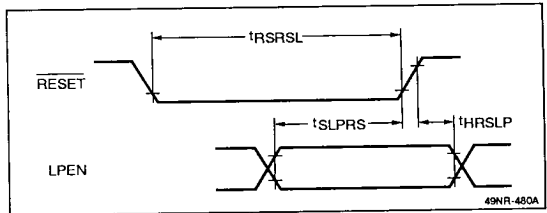
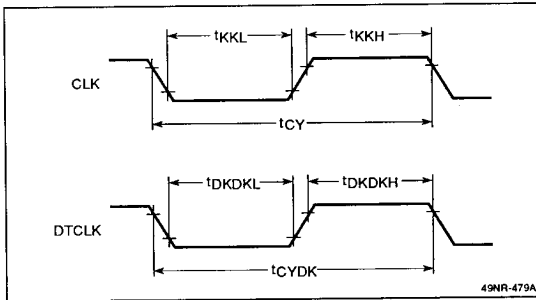
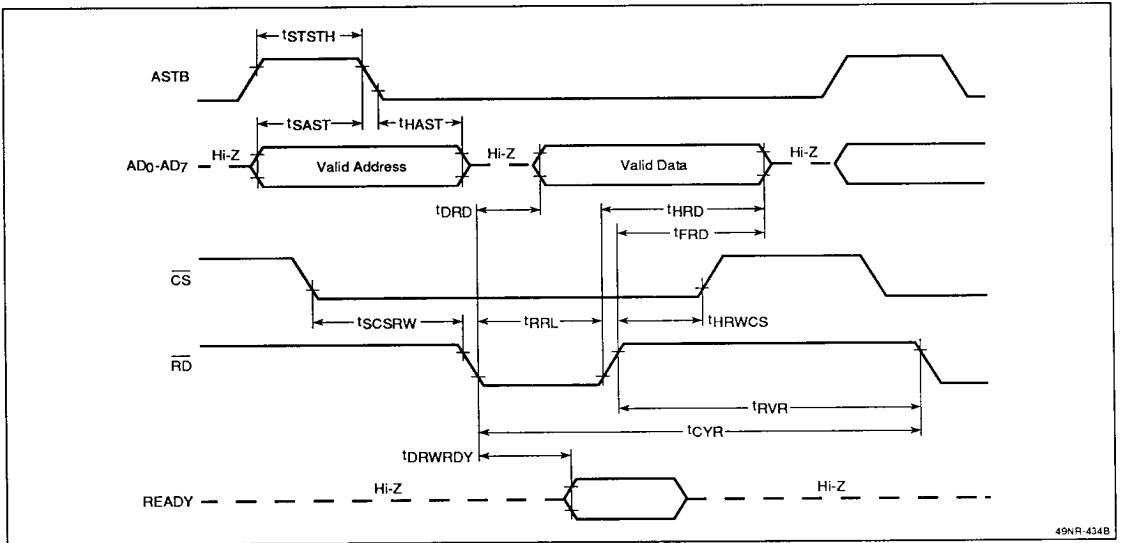


Figure 2. Clock Waveform



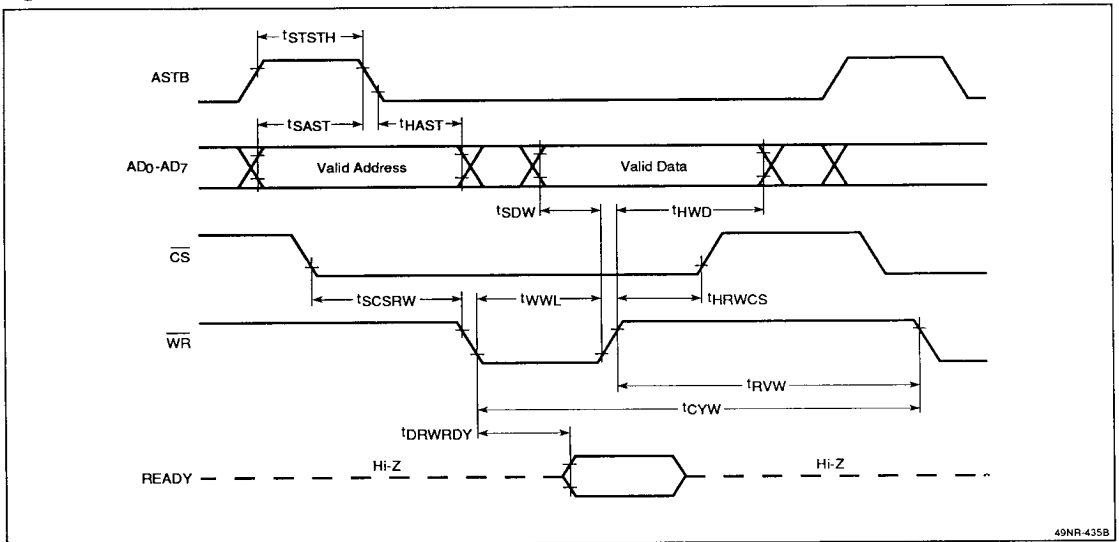
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Figure 4. CPU Read Cycle



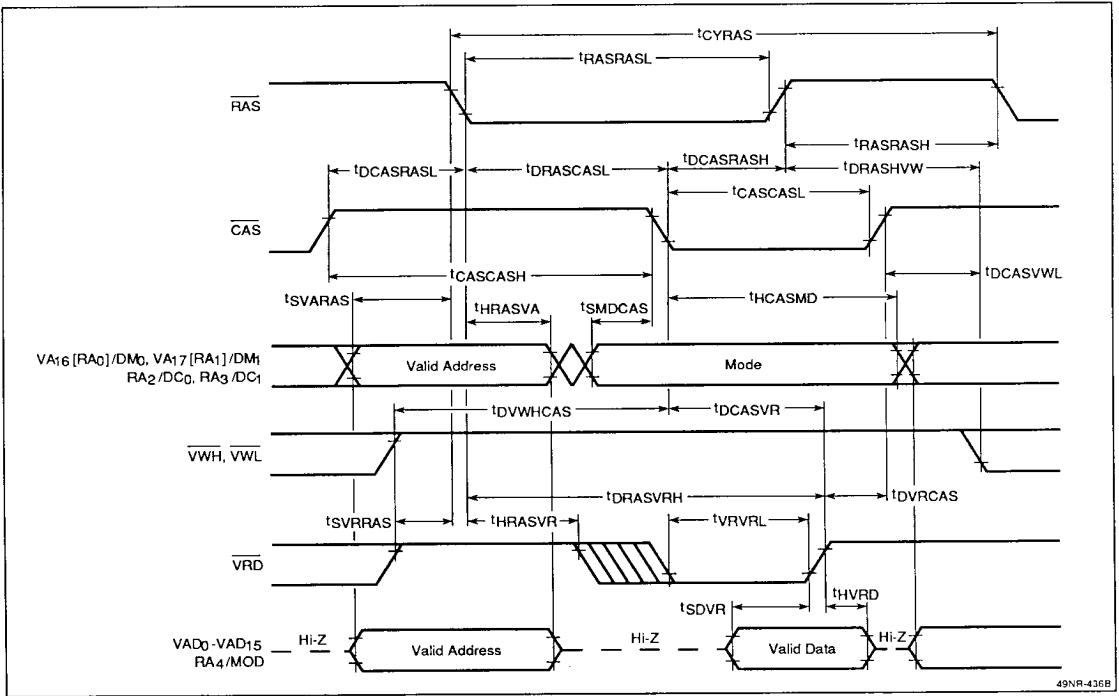
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Figure 5. CPU Write Cycle



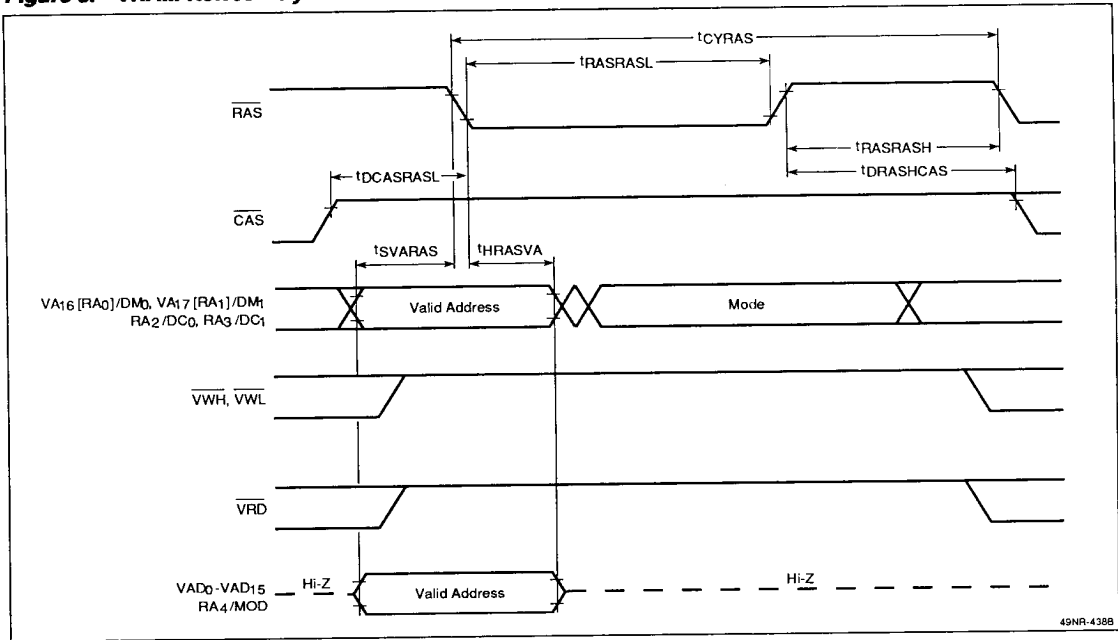
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Figure 6. VRAM Read Cycle



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Figure 8. VRAM Refresh Cycle



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Figure 9. VRAM Request; Interleave Mode

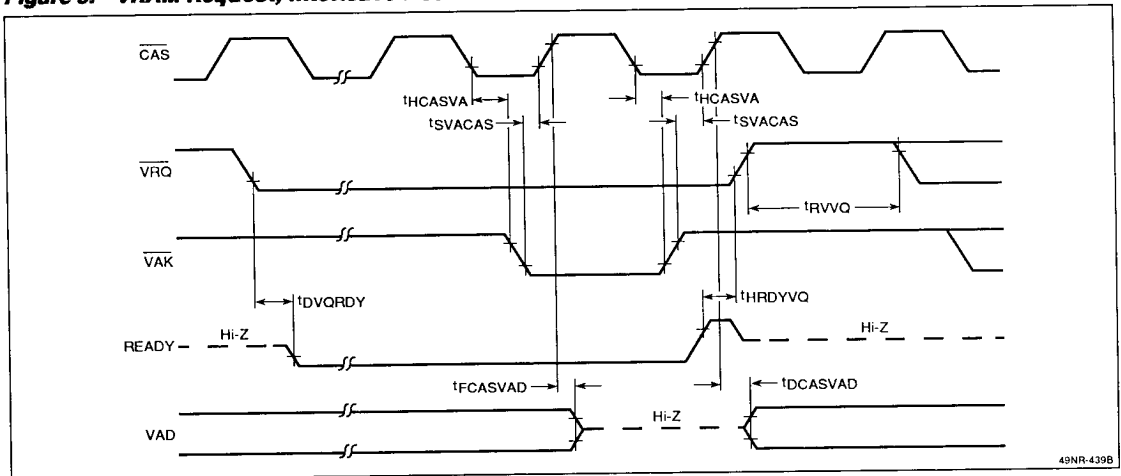


Figure 10. VRAM Request; Dual-Port Mode

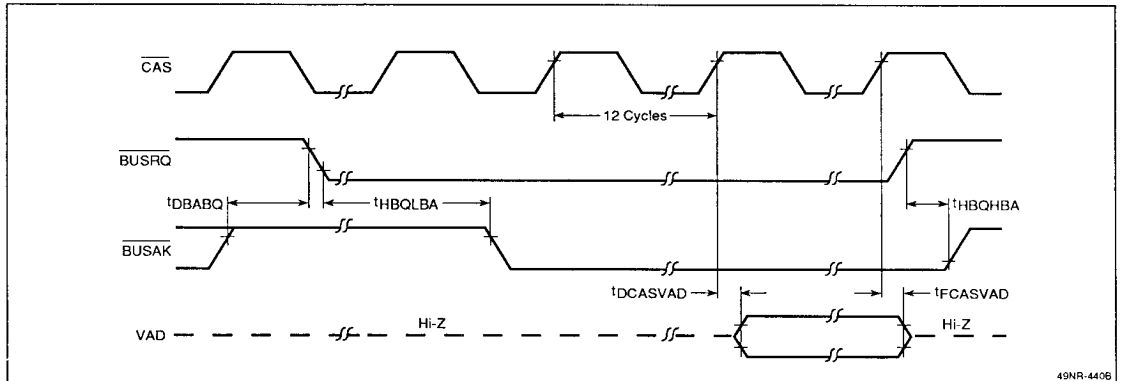
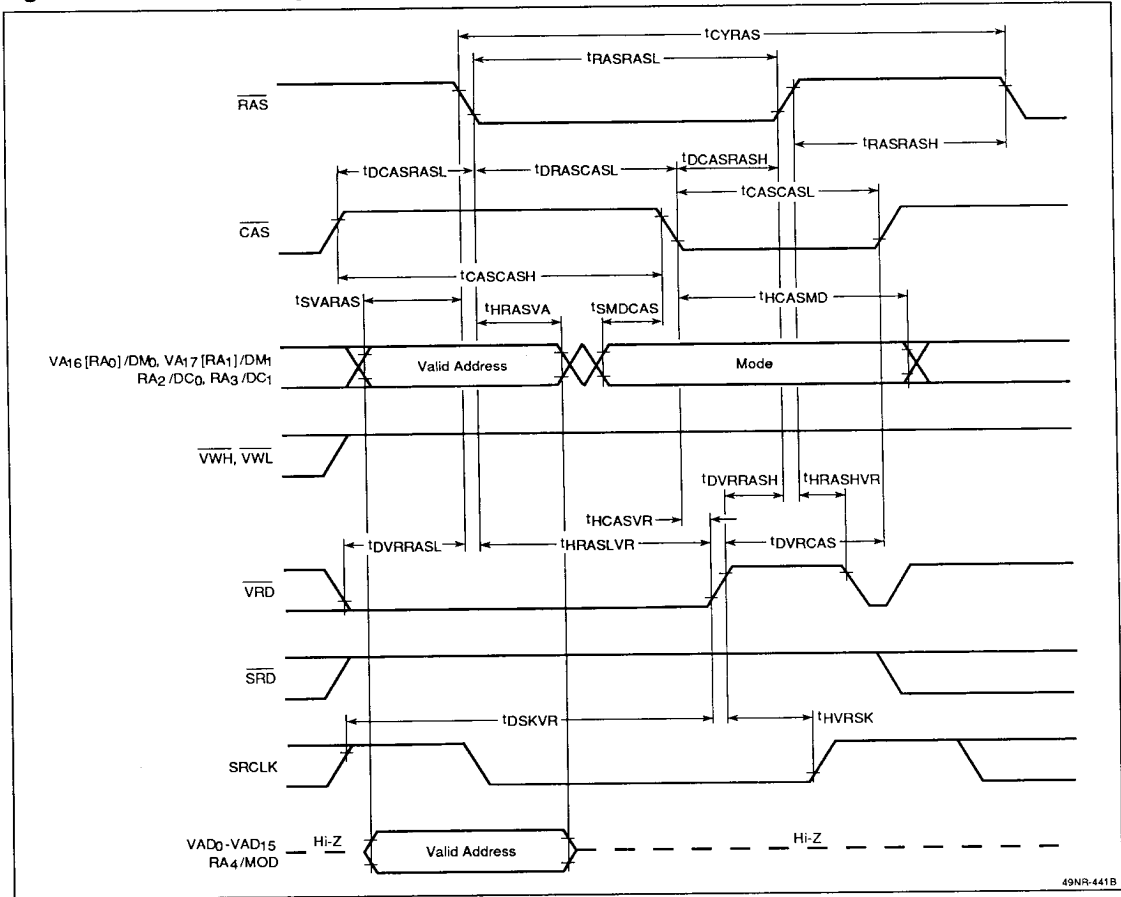
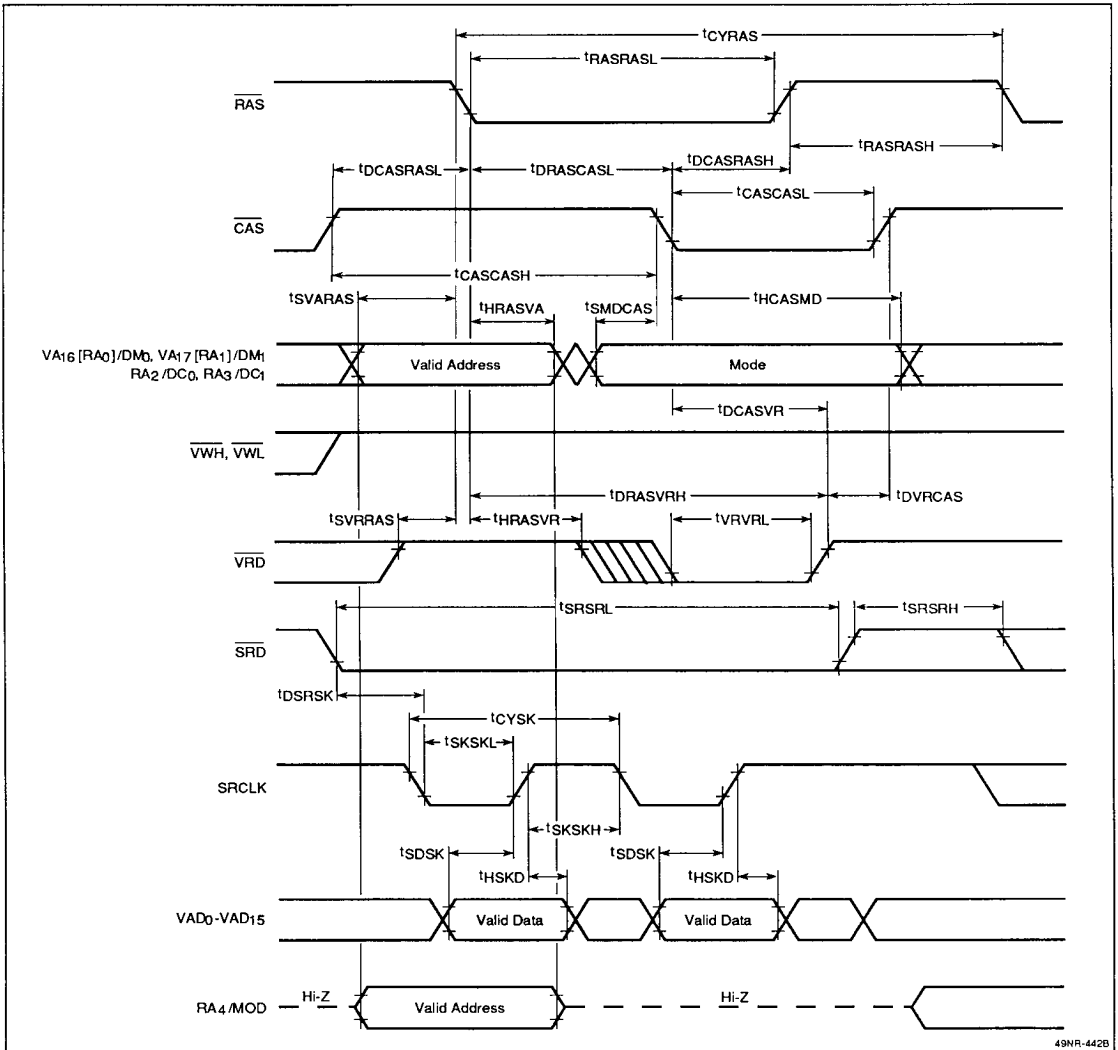


Figure 11. Data Transfer Cycle



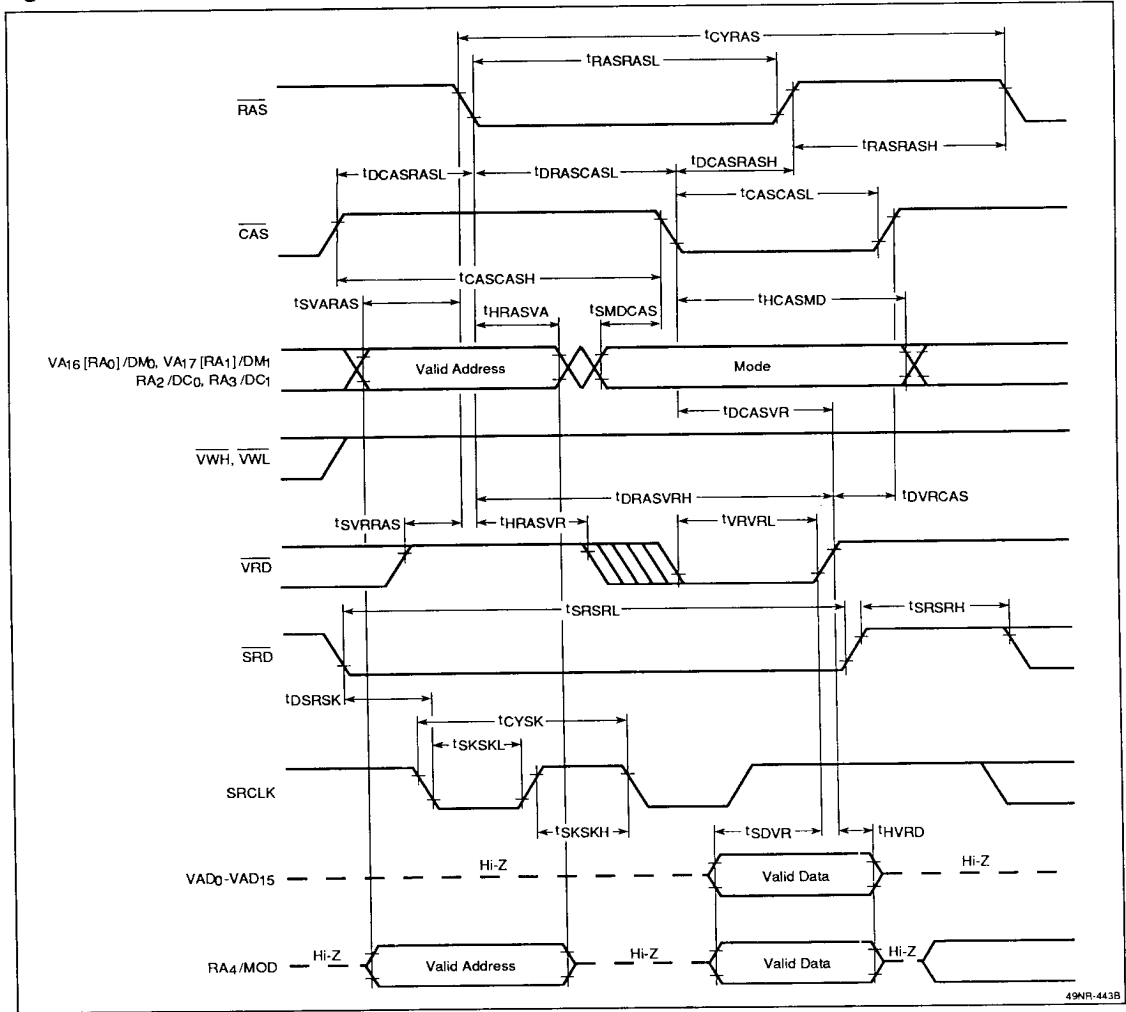
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Figure 12. VRAM Serial Read Cycle; Graphics Display



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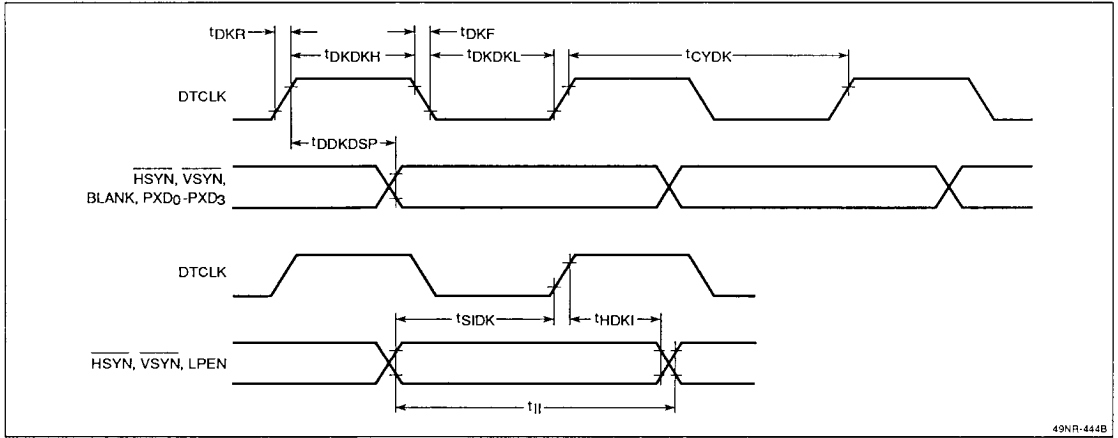
Figure 13. VRAM Serial Read Cycle; Text or Semigraphics Display



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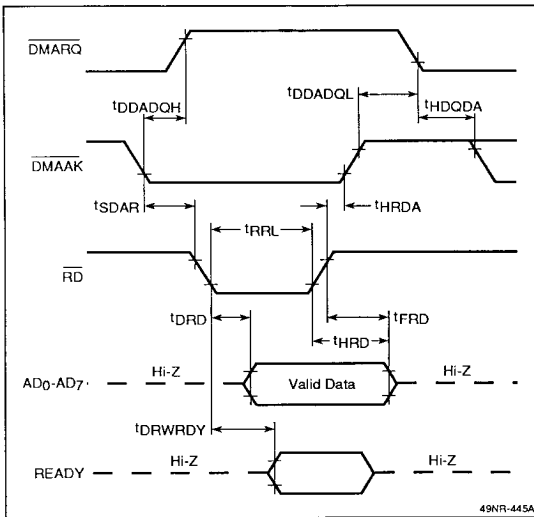
49NR-443B

Figure 14. Display Timing



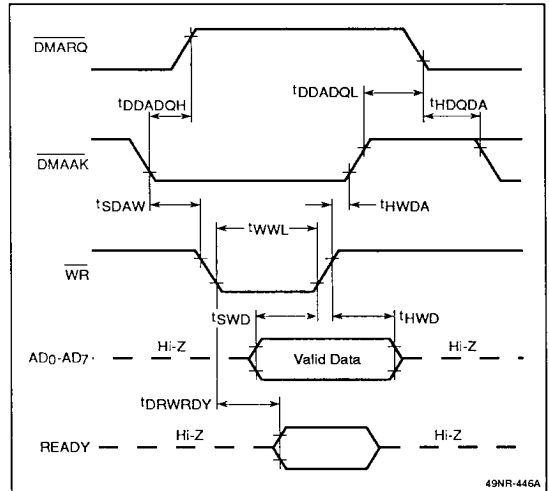
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Figure 15. DMA Read Cycle



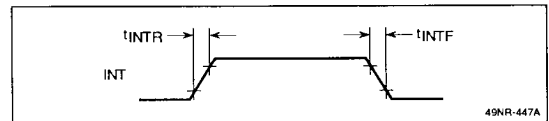
49NR-445A

Figure 16. DMA Write Cycle



49NR-446A

Figure 17. Interrupt Waveform



49NR-447A

INTERNAL STRUCTURE

The μPD72022 IDP consists of three units: host processor interface unit, control processor unit, and display control unit. Refer to the μPD72022 Block Diagram.

Host Processor Interface Unit

The host processor interface unit transfers commands, parameters, and such status information as the μPD72022 internal processing state, to and from the host processor.

Control functions include asynchronous bus interface control, DMA control, and interrupt control.

Control Processor Unit

The control processor unit reads and executes commands and parameters from the host processor via the host processor interface unit.

Display data processing in video memory, display address control, screen control, etc., in the display control unit are implemented.

Display Control Unit

The display control unit generates and outputs video memory display addresses, display signals, and CRT control signals. It generates various timing signals required in the μPD72022.

COMMANDS

The μPD72022 has 22 commands for implementing initialization, display control, and sprite control operations. See table 2.

Table 2. List of Commands

Name	Function
Initialization	
SYNC	Selects display operation mode and specifies scan timing.
Display Control	
DSPOF	Generates screen control table base address and border color; enables display controller; starts display.
DSPOP	Disables display controller and terminates display.
DSPDEF	Defines display screen layout and display format.
CURDEF	Defines cursor display format.
ACTSCR	Selects active screen area.
CURS	Moves cursor to specified cursor display position.
LPNR	Determines light pen position.

Table 2. List of Commands (cont)

Name	Function
Video Memory Control	
DPLD	Specifies video memory operation address or address offset.
DPRD	Determines video memory operation address.
MASK	Sets bit mask for data storage in video memory.
RDAT	Reads contents of video memory and sends data to host processor.
WDAT	Stores transfer data in video memory.
BLKTOT	Reads the video memory contents and transfers the data via DMA operation.
BLKTIN	Stores the data transferred via DMA operation into the video memory.
EXIT	Terminates video memory operation command processing.
Sprite Control	
SPRON	Enables the sprite controller and initiates sprite image display.
SPOF	Disables the sprite controller and terminates sprite image display.
SPRSW	Toggles the sprite display on or off for each sprite operation.
SPR RD	Reads the sprite attribute table data.
SPRWR	Writes data into the sprite attribute table.
SPOV	Determines the sprite controller operation status.

INITIALIZATION COMMANDS

SYNC Command

Command Code 10H

0	0	0	1	0	0	0	0
---	---	---	---	---	---	---	---

Parameters

RM		EL	EV	VM	0	DPM	ILM
0	RF	EC	ES	FV	RS		
0	0	LBR					
0	0	LBR					
HAD							
0	0	RBR					
0	0	RBL					
0	0	HS					
0	0	TBL					
0	0	TBR					
VAD (L)							
0	VAD (H)	BBR					
0	0	BBL					
0	0	VS					

The SYNC command terminates display controller operation and defines operation mode and horizontal/vertical scan timing with the following parameters.

- **ILM, DPM** (Interleave Mode, Dual Port Mode)

The format of the interblock interface between the host system, IDP, and video memory is specified. Dual-port mode can only be specified for the VRAM serial access (VM = 1).

DPM	ILM	Operation
0	0	Standalone mode
0	1	Interleave mode
1	0	Dual-port mode
1	1	Disabled

- **EV** (Enable Vertical Blank Interrupt)

Parameter EV determines whether the occurrence of a vertical blanking signal causes an interrupt signal to be generated on the INT pin.

EV Interrupt

- 0 Vertical blank interrupt disabled
- 1 Vertical blank interrupt enabled

- **EL** (Enable Light Pen Interrupt)

Parameter EL specifies whether the occurrence of a light-pen signal causes an interrupt signal to be generated on the INT line.

EL Interrupt

- 0 Light pen interrupt disabled
- 1 Light pen interrupt enabled

- **VM** (VRAM Access Mode)

Parameter VM specifies the video memory access mode for static picture display data generation.

VM Video Memory

- 0 Random access mode
- 1 Serial access mode

- **RM** (Raster Mode)

Parameter RM specifies CRT scanning mode and display signal generation mode.

RM CRT Scanning Mode

- 00 Noninterlace (640 x 400, 24K CRT)
- 01 Interlace (640 x 400, 15K CRT)
- 10 Vertical magnify (640 x 200, 24K CRT)
- 11 Normal (640 x 200, 15K CRT)

- **RS** (Resolution Select)

Parameter RS specifies the divide ratio for generation of the display signal dot time. This ratio can be combined with horizontal and vertical scan timing to vary display resolution. Table 3 is an example based on a 20-MHz source clock.

Table 3. Display Resolution Example (20-MHz Clock)

RS	Divide Ratio	Corresponding Resolution	HAD Setup Value	VAD Setup Value	Recommended CRT
000	Divide by 4	256 x 192	256 (63)	192	Horizontal scan frequency 15.75 kHz
001	Divide by 3	320 x 200	320 (79)	200	
010	Divide by 2	512 x 192	512 (127)	192	
011	Divide by 1.5	640 x 200	640 (159)	200	
100	Divide by 1	640 x 400	640 (159)	400	24.83 kHz
Others	Disabled (dot clock is not output)				

● **RV (Reverse Screen)**

Parameter RV specifies reverse display of the entire screen. When RV is cleared to 0, normal display is enabled; when RV is set to 1, text foreground and background colors in the text display are reversed.

● **ES (External Sync)**

Parameter ES specifies use of the $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$ pins and external synchronization. When ES is set to 1, horizontal and vertical synchronizing signals are output on the $\overline{\text{HSYN}}$ and $\overline{\text{VSYN}}$ pins.

When ES is cleared to 0, the pins are placed in a high-impedance state, and display timing is synchronized with an input reference signal.

● **EC (External Clock)**

Parameter EC specifies DTCLK pin operation and determines display timing signals. When EC is set to 1, a signal generated from the internal divider is output on the DTCLK pin as dot clock.

When EC is cleared to 0, the DTCLK pin is placed in a high-impedance state, and display timing is based on an input clock reference signal.

EC can be set in external dot clock input mode (LPEN signal is low at reset time).

● **RF (Refresh Control)**

Parameter RF controls video memory refresh operations. When RF is cleared to 0, no refresh operation is performed; when set to 1, refresh operations are initiated.

● **LBL (Left Blanking)** See figure 18.

- LBR (Left Border)**
- HAD (Horizontal Active Display)**
- RBR (Right Border)**
- RBL (Right Blanking)**
- HS (Horizontal Sync)**

Horizontal scan timing is specified in four-dot time (TCK) units. Each timing is generated at the time of (specified value + 1) x TCK.

The horizontal scan parameters have the following restrictions.

- $\text{HS} \geq 04\text{H}$
- $\text{LBL} \geq 03\text{H}$
- $\text{HAD} = \text{odd number (bit 0} = 1)$

● **TBL (Top Blanking)** See figure 18

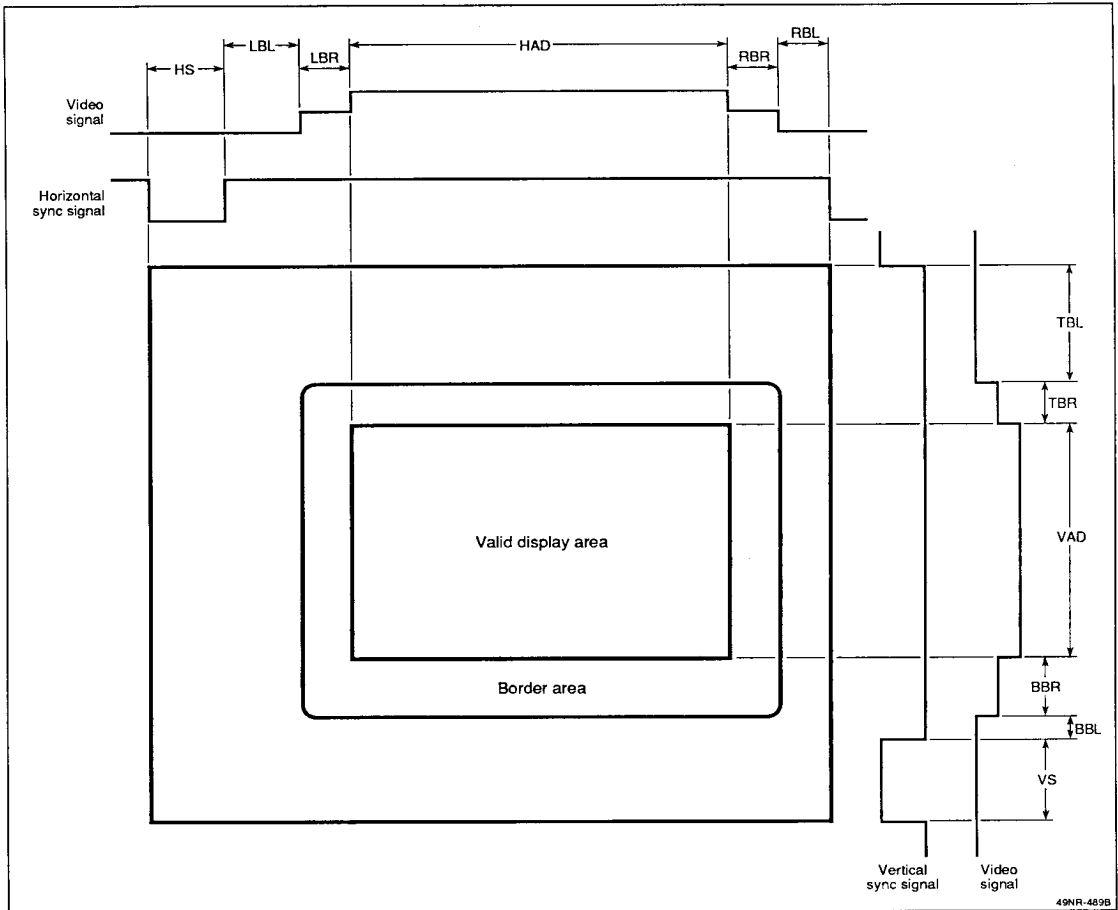
- TBR (Top Border)**
- VAD (Vertical Active Display)**
- BBR (Bottom Border)**
- BBL (Bottom Blanking)**
- VS (Vertical Sync)**

The number of rasters (vertical scan lines) is specified to control vertical scan timing. An integer multiple of 2 is set in the valid display time (VAD). The vertical border time (TBR, BBR) can be omitted if the specified value is 0.

The vertical scan parameters have the following restrictions.

- $\text{VS} \geq 04\text{H}$
- $\text{TBL} + \text{TBR} \geq 10\text{H}$ (for non-sprite display)
- $\text{TBL} + \text{TBR} \geq 20\text{H}$ (for sprite display)
- $\text{VAD} \geq 04\text{H}$
- $\text{BBR} + \text{BBL} \geq 02\text{H}$

Figure 18. Horizontal and Vertical Scan Parameters



49NR-489B

DISPLAY CONTROL COMMANDS

DSPON Command

Command Code 12H

0	0	0	1	0	0	1	0
---	---	---	---	---	---	---	---

Parameters

Base address					(lower)
0	0	0	0	0	(upper)
0	0	0	0	0	BC

The DSPON command enables the display controller and generates the display signal.

In display access after the screen control table base address is specified in byte units, the address provided by multiplying the setup value by 256 is referenced as the screen control table start address.

● **BC (Back Drop Color)**

Parameter BC specifies the background color of the transparent color specification portion of the valid display time and the horizontal/vertical border area.

DSPOF Command

Command Code 13H

0	0	0	1	0	0	1	1
---	---	---	---	---	---	---	---

The DSPOF command disables the display controller and sprite controller and terminates display. The horizontal/vertical retrace time is output on the display signal output pin.

DSPDEF Command

Command Code 14H

0	0	0	1	0	1	0	0
---	---	---	---	---	---	---	---

Parameters

ATROFF (L)							
ATROFF (M)							
0	PITCH			0	(H)		
0	0	0	MRA				
0	0	0	HRA				
BR				0	0	0	

The DSPDEF command defines display screen layout and display format. The following parameters are specified.

- **ATROFF** (Attribute Offset)

The character code and attribute code store address offset are specified in byte units. If the offset is a negative value, input the complement.

<u>ATROFF</u>	<u>Offset</u>
0H	Disabled
1H	1 byte
2H	2 bytes
:	:
3FFFFH	262,143 bytes
40000H	-262,144 bytes
:	:
7FFFFH	-1 byte

- **PITCH** (Character Pitch)

The character code pitch is specified.

<u>PITCH</u>	<u>Pitch</u>
0H	Disabled
1H	1 byte
:	:
7H	7 bytes

- **MRA** (Maximum Raster Address)

The character vertical display size is specified in number of rasters. This position is used as the under-line display position.

<u>MRA</u>	<u>No. of Rasters</u>
0 to 6H	Disabled
7H	8 rasters
:	:
1FH	32 rasters

- **HRA** (Horizontal Raster Address)

The horizontal line display position is specified as a raster position.

<u>HRA</u>	<u>Display Position</u>
0H	First raster
1H	Second raster
:	:
1FH	32nd raster

- **BR (Blinking Rate)**

The blink attribute character display and cursor blink are specified. Each character specified with the blink attribute is turned on (bright) in the time of the setup value x 24 fields and off (dark) in the time of the setup value x 8 fields.

The cursor blinks in the time of the setup value x 8 fields.

The number of bright and dark fields for attribute and cursor blink are shown below.

BR	Attribute		Cursor	
	Bright	Dark	Bright	Dark
0H	768	256	256	256
1H	24	8	8	8
2H	48	16	16	16
:	:	:	:	:
1FH	744	248	248	248

- **CURDEF Command**

Command Code 15H

0	0	0	1	0	1	0	1
---	---	---	---	---	---	---	---

Parameters

CURN	0	CE	BE
------	---	----	----

The CURDEF command defines the cursor display mode. Parameter CURN specifies cursor sprite, and the CURS command specifies the cursor position, which also updates the display position of the sprite specified in CURN.

- **BE (Blinking Enable)**

Parameter BE specifies whether cursor blinking is enabled. To suppress cursor blinking, clear BE to 0.

- **CE (Cursor Enable)**

Parameter CE specifies whether cursor display is enabled. To turn off the cursor, clear CE to 0.

Since the sprite function is used for cursor display, specify sprite display accordingly at the same time.

- **ACTSCR Command**

Command Code 16H

0	0	0	1	0	1	1	0
---	---	---	---	---	---	---	---

Parameters

0	SCRN	0	0	0	0	0
---	------	---	---	---	---	---

The active screen area where cursor position control and light pen position control are valid is specified.

- **SCRN Active Screen Area**

0	First split screen
1	Second split screen
2	Third split screen
3	Fourth split screen

- **CURS Command**

Command Code 1EH

0	0	0	1	1	1	1	0
---	---	---	---	---	---	---	---

Parameters

Vertical position (lower)							
0	0	0	0	0	(upper)		
Horizontal position (lower)							
0	0	0	0	0	(upper)		

The cursor is moved to the position specified by the parameters.

Screen position is specified by virtual screen coordinates, first designating a Y (line) position value, then an X (column) position value. If a specified position exceeds the lower or right edge of the virtual screen, the cursor is positioned at the respective edge of the virtual screen.

The internal variable data pointer (DPTR0) is updated to the video memory address value corresponding to the coordinates of the cursor position.

LPNR Command

Command Code 1AH

0	0	0	1	1	0	1	0
---	---	---	---	---	---	---	---

Output Data

Vertical position (lower)						(upper)
0	0	0	0	0		
Horizontal position (lower)						(upper)
0	0	0	0	0	0	

The light pen detection coordinates are determined and the light pen detection status is reset to 0.

Virtual screen coordinates are specified by first designating the Y (line) position and then the X (column) position.

The internal variable data pointer (DPTR0) is updated to the video memory address value corresponding to the light pen detection coordinates.

VIDEO MEMORY OPERATION COMMANDS

DPLD Command

Command Code 8E/8FH

1	0	0	0	1	1	1	N
---	---	---	---	---	---	---	---

Parameters

VRAM address (lower)						(upper)
(intermediate)						
0	0	0	0	0		

The address data entered by using the parameter is stored in the specified internal variable data pointer (DPTR0 or DPTR1)

N	Data Pointer
0	Store in DPTR0
1	Store in DPTR1

The data pointer value is used for address specification or update in later VRAM access.

The 19-bit address parameter can be used to access 512K-byte video memory space. If the DPTR1 value is negative, input the complement.

In the commands listed in table 4, the address update mode is specified in the command code MOD field, and the data pointer value can be updated each time a VRAM access is made.

If the coordinates on the virtual screen can be obtained by cursor position specification and light pen input position detection, the data pointer (DPTR0) is updated to the corresponding video memory address value.

Table 4. Data Pointer Update

MOD	Data Pointer Update	RDAT, WDAT	BLKTOT, BLKTIN
00	Data pointer is not changed.	Enabled	Disabled
01	ATROFF value is added; then the data pointer is updated.	Enabled	Enabled
10	PITCH value is added; then the data pointer is updated.	Enabled	Enabled
11	DPTR1 value is added; then the data pointer is updated.	Enabled	Enabled

DPRD Command

Command Code 8AH

1	0	0	0	1	0	1	0
---	---	---	---	---	---	---	---

Output Data

VRAM address (lower)						(upper)
(intermediate)						
0	0	0	0	0		

The data pointer (DPTR0) value is determined.

MASK Command

Command Code 89H

1	0	0	0	1	0	0	1
---	---	---	---	---	---	---	---

Parameters

Mask data							
-----------	--	--	--	--	--	--	--

The mask data entered via the parameter is stored in the internal variable mask register (MSKR).

The mask register value is used for write data mask processing in later VRAM access. When the mask bit value is 0, the VRAM contents are held; when 1, write data is stored.

In mask processing, the mask register value is determined before a VRAM write operation is initiated.

The video memory contents at the transfer destination address are read and ANDed with the inverted mask data value, and a mask is set. In addition, the write data to be stored in video memory and the mask data value are ANDed together, and a mask is set. The results are ORed together, and then written into video memory.

RDAT Command

Command Code 90/91/92/93H

1	0	0	1	0	0	MOD
---	---	---	---	---	---	-----

Output Data

Read data
·
·
·
Read data

The video memory contents are read from the address specified in the data pointer (DPTR0), and the data is transferred to the host processor.

If the host processor receives the memory data, the data pointer (DPTR0) contents are updated according to MOD specification (table 4), and the video memory contents at the next address are read and transferred.

The memory contents are read until another command is entered.

WDAT Command

Command Code 94/95/96/97H

1	0	0	1	0	1	MOD
---	---	---	---	---	---	-----

Input Data

Write data
·
·
·
Write data

With the WDAT (Write VRAM Data) command, mask processing is performed for data input by the host processor according to the mask register value. Then, the data is written into video memory at the address specified by the data pointer (DPTR0).

After the data is written, the data pointer (DPTR0) contents are updated according to MOD specification (table 4) to the next video memory address.

If the host processor inputs data consecutively, the data write into video memory and data pointer update are repeated until another command is entered.

BLKTOT Command

Command Code 99/9A/9BH

1	0	0	1	1	0	MOD
---	---	---	---	---	---	-----

DMA Transfer Output Data

Read data
·
·
·
Read data

The video memory contents are read from the address specified in the data pointer (DPTR0) and stored in the output data buffer. A DMA transfer request signal (DMARQ) is then generated to prompt the DMA controller to receive the read data. The DMA acknowledge signal (DMAAK, RD) is used to output the data buffer contents to the data bus. If the DMA controller receives the data and the buffer is not empty, the DMA transfer request generation is continued.

If the buffer is empty, the data pointer (DPTR0) value is updated according to MOD specification (table 4), and the video memory contents at the next address are read and stored in the output data buffer. Therefore, the address of the data read by the DMA controller does not correspond to the data pointer value.

If the output data buffer is empty, the memory read and the data pointer update are repeated until the host processor inputs another command based on the DMA controller terminal count.

BLKTIN Command

Command Code 9D/9E/9FH

1	0	0	1	1	1	MOD	
---	---	---	---	---	---	-----	--

DMA Transfer Input Data

Write data							
·							
·							
·							
Write data							

DMA transfer request signal (DMARQ) is generated to prompt the DMA controller to transfer write data. Data input together with the DMA acknowledge signal (DMAAK, WR) is written into video memory.

Mask processing is performed for data input by executing the DMA transfer according to the mask register value; then the data is written into video memory at the address specified in the data pointer (DPTR0).

After the data is written, the data pointer (DPTR0) contents are updated according to MOD specification (table 4) to the next video memory address.

If the DMA controller inputs data consecutively, the data write into video memory and the update of the data pointer are repeated until the host processor inputs another command based on the DMA controller terminal count.

EXIT Command

Command Code 88H

1	0	0	0	1	0	0	0
---	---	---	---	---	---	---	---

Command processing during parameter acceptance is stopped and a command wait state is initiated.

Video memory operation command processing during data transfer is stopped and a command wait state is initiated.

If parameter acceptance is terminated and processing is started, data or any command other than the video memory operation commands cannot be terminated by issuing the EXIT command.

SPRITE CONTROL COMMANDS

SPRON Command

Command Code 82H

1	0	0	0	0	0	1	0
---	---	---	---	---	---	---	---

Parameters

SAB (lower)										
0	0	0	0	0	(upper)					
HSPN					ESP	SPMG	SPGR			

If the display controller has been enabled by the DSPON command, sprite display is initiated.

The sprite status (SC) in the status data is reset and interrupt signal generation from the sprite controller is enabled or disabled according to ESP specification.

The sprite attribute table and sprite pattern area base address (SAB), sprite magnification (SPMG), and sprite grouping function (SPGR) are set in the sprite controller.

If the command is input during sprite display, the sprite controller operation parameter is changed.

- **HSPN** (Horizontal Sprite Number)

This parameter specifies the maximum number of sprite images that can be displayed on a single horizontal line.

- **SPMG** (Sprite Magnify)

Sprite magnification display is specified. When SPMG is set to 1, sprite display data is magnified two-fold in the vertical direction display.

- **SPGR** (Sprite Grouping)

The grouping function in sprite detection is specified. When SPGR is set to 1, collision detection between different groups is enabled.

- **ESP** (Enable Sprite Interrupt)

INT signal from the sprite controller is specified. When ESP is set to 1, an INT signal is generated at the INT pin when sprite collision is detected or the maximum number of sprite images is exceeded.

SPROF Command

Command Code 83H

1	0	0	0	0	0	1	1
---	---	---	---	---	---	---	---

Sprite controller operation is disabled and sprite display is terminated.

SPRRD Command

Command Code 80H

1	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---

Parameters

SPN	ATN
-----	-----

Output Data

Read data 1
·
·
·
Read data n

The sprite attribute table contents are read from the address corresponding to the SPN (sprite number) and ATN (attribute number) parameters, and the data is transferred to the host processor.

ATN	Attribute
0	YP lower
1	YSIZE, SPSW, YP upper
2	XP lower
3	XSIZE, SPDM, XP upper
4	SPDA lower
5	SPDA upper
6	SCF (color)
7	Not used

If the host processor receives the attribute data, the attribute number is incremented and the next attribute data is read and transferred. When attribute number 7 is read, the sprite number is also updated so that the next sprite vertical position (YP lower) can be read.

The attribute data read and the attribute and sprite number update are repeated until another command is input.

SPWR Command

Command Code 84H

1	0	0	0	0	1	0	0
---	---	---	---	---	---	---	---

Parameters

SPN	ATN
-----	-----

Input Data

Store data 1
·
·
Store data n

Data input by using the parameters is stored in the sprite attribute table.

ATN	Attribute
0	YP lower
1	YSIZE, SPSW, YP upper
2	XP lower
3	XSIZE, SPDM, XP upper
4	SPDA lower
5	SPDA upper
6	SCF (color)
7	Not used

The input data following the second parameter is written into video memory from the address corresponding to the first parameter SPN (sprite number) and ATN (attribute number).

Each time one byte of data is stored, the attribute number is incremented so that the next attribute number can be specified. When attribute number 7 is stored, the sprite number is also updated so that the next sprite vertical position (YP lower) can be specified.

If the host processor inputs data consecutively, the attribute number is incremented from 0 through 7 for each sprite number, which advances in increments of 1.

SPRSW Command

Command Code 85H

1	0	0	0	0	1	0	1
---	---	---	---	---	---	---	---

Parameters

SPN	0	SPSW	0
-----	---	------	---

This command specifies the sprite display on or off by setting the sprite attribute SPSW bit.

The sprite number is specified in the SPN parameter. If the SPSW parameter is set to 1, sprite display is turned on; if cleared to 0, sprite display is turned off. Thus, display on or off for each sprite can be specified as desired.

SPROV Command

Command Code 81H

1	0	0	0	0	0	0	1
---	---	---	---	---	---	---	---

Output Parameters

0	SO	C	OVS
---	----	---	-----

The sprite controller operation status is determined and the sprite status bit in the status data (SC) is reset to 0.

The sprite controlled status is defined by parameters SO, OVS, and C.

- (1) SO indicates whether the maximum number of sprite images that can be displayed on a single horizontal line (HSPN specification) has been exceeded.
- (2) OVS specifies the first excessive sprite number.
- (3) C indicates the detection of sprite collision.

STATUS

The μPD72022 sends the display hardware operation status and command processing status information to the host processor via the status output port.

The status data format and the bit contents viewed from the host are explained below.

7	6	5	4	3	2	1	0
LP	VB	SC	ER	—	BUSY	OBF	IBF

Input Buffer Full

IBF (bit 0) indicates that data is stored in the internal input data buffer during command/parameter input from the host processor. It is set on the rising edge of the WR strobe signal when the host processor writes commands/parameters. It is reset when the input data buffer contents are read by μPD72022 internal processing.

The host processor should check that the flag is reset before inputting the next command/parameter. If a command/parameter is input when the flag is set, the μPD72022 drives the READY signal low, forcing the host to wait.

Output Buffer Full

OBF (bit 1) indicates that the μPD72022 has data stored in the output data buffer. It is set when a write is made to the output data buffer during internal processing. It is reset on the rising edge of the RD strobe signal when the host reads the output data buffer contents through the parameter output port.

The host processor should check that the flag is set before reading data from the parameter output port. If data is read when the flag is set, the μPD72022 drives the READY signal low, forcing the host to wait. The flag is reset when a command is input.

Busy

The BUSY flag (bit 2) indicates that the μPD72022 is performing command processing. It is set under the same conditions as IBF and reset when the execution of all commands stored in the internal FIFO buffer has been completed.

In command processing of SPRRD, SPRWR, BLKTIN, BLKTOT, WDAT, or RDAT, however, BUSY is reset when the FIFO buffer is empty after the completion of processing of successive input commands. Therefore, BUSY is always set when any of these six commands is being executed.

Error

ER (bit 4) indicates that an error occurred during command processing. It is set when an abnormal state is encountered; for example, when parameters required for command execution are not entered, or the value of an entered parameter is not proper.

When an error occurs, μPD72022 stops command processing. To recover, issue the EXIT command, followed by the desired command. ER is reset when the EXIT command is executed.

Specific error causes are as follows.

- (1) Parameter is entered when command code is not entered.
- (2) Command/parameter is entered from any port other than the command or parameter input port.
- (3) Any code other than a command code is entered from the command port.

- (4) The number of parameters is too large. Up to a given number of parameters are assumed to be valid and processed. When excessive parameters are entered, ER is set and the excessive parameters are not processed.
- (5) The number of parameters is too small. All the entered parameters are assumed to be valid and processed.
 - (a) When a command (except EXIT) is entered following the parameters, ER is set and command processing starts
 - (b) When an EXIT command is entered following the parameters, it is assumed that termination of the immediately preceding command entered is specified. ER is not set and command entry is awaited.
 - (c) When other than a command or parameter entry follows the parameters, an error results. ER is set and command entry is awaited.
- (6) LPNR command is made on any area other than the active screen area specified by the ACTSCR command.

Sprite Control

The SC flag (bit 5) indicates occurrence of sprite over or sprite collision state during sprite display operation. It is updated each time one screen display is terminated (vertical blank).

- (1) Sprite Over. The SC flag is set when the number of

sprite images existing on a single horizontal line exceeds the HSPN setup value. The first sprite number exceeding the setup value can be read by command (SPROV) specification.

- (2) Sprite Collision. The SC flag is set when dot overlap of two or more sprite images occurs.

Vertical Blank

VB (bit 6) indicates vertical blanking time (BBR, BBL, or VS time). It can be used for the host processor to synchronize with display operations.

Light Pen Detect

LP (bit 7) indicates that an address is detected by using the light pen signal. It is set when the address is detected and reset when the LPNR command is issued.

CONTROL

After initialization (figure 19), the μPD72022 executes control according to the sequence shown in figure 20.

In figure 20, a check is made to ensure that IBF (bit 0) of the μPD72022 status data format is cleared to 0; then the command/parameter is written.

If the command is a data read or write command, then data is read or written.

The sequence to check that the IBF bit is cleared to 0 can be omitted by using the READY signals; however, this does not apply to read commands (RDAT, BLKTOT, SPRRD, DPRD, LPNR, SPROV).

Figure 19. μPD72022 Initialization

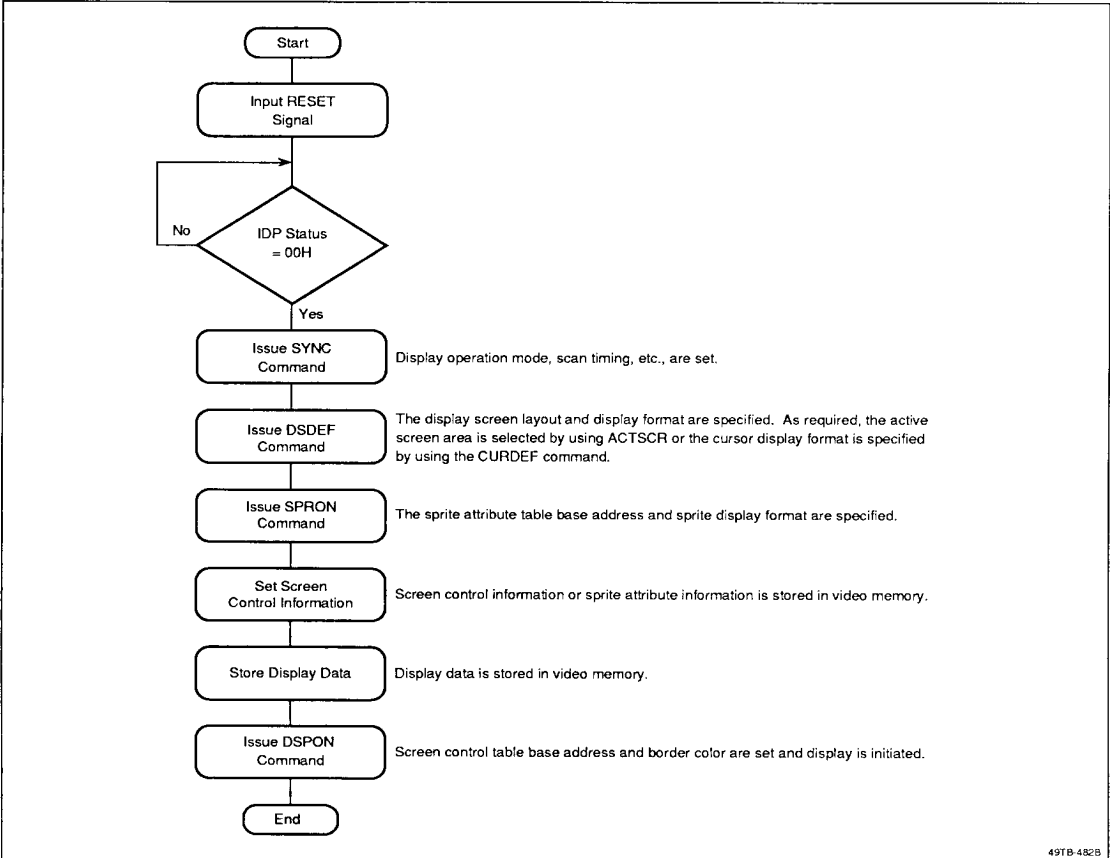
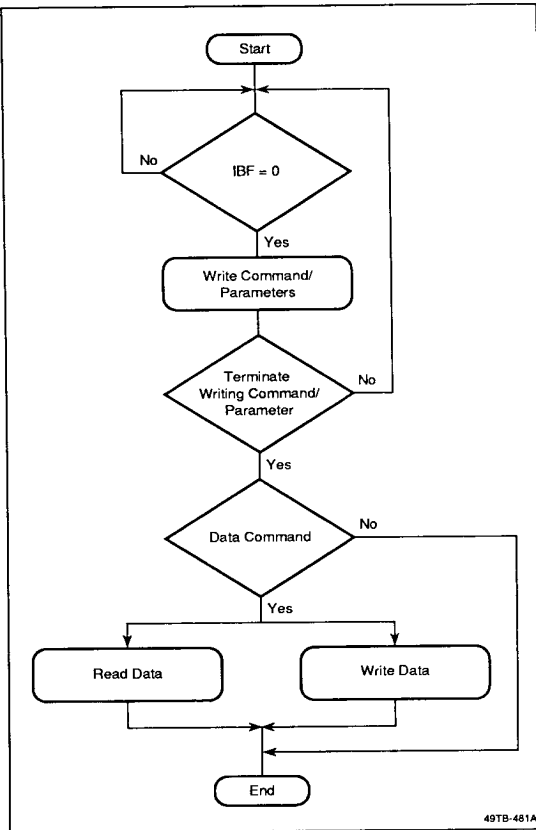


Figure 20 μPD72022 Basic Control Flow



DISPLAY

Static Picture Display

The μPD72022 IDP has three static picture display modes: text, semigraphics, and graphics.

Text Mode. Video memory data is recognized as character code and attribute data. Character patterns from the character generator specified by character code are displayed. Color or format qualification is specified by attribute data paired with character code. See figure 21.

Semigraphics Mode. Video memory data is recognized as pattern code. Pattern data (format and color) in the pattern data area specified by pattern code is displayed. Two modes are available according to how pattern data is stored. See figures 22 and 23.

Graphics Mode. Video memory data is recognized and displayed as color patterns corresponding directly to the display screen. See figure 24.

Sprite Image Display

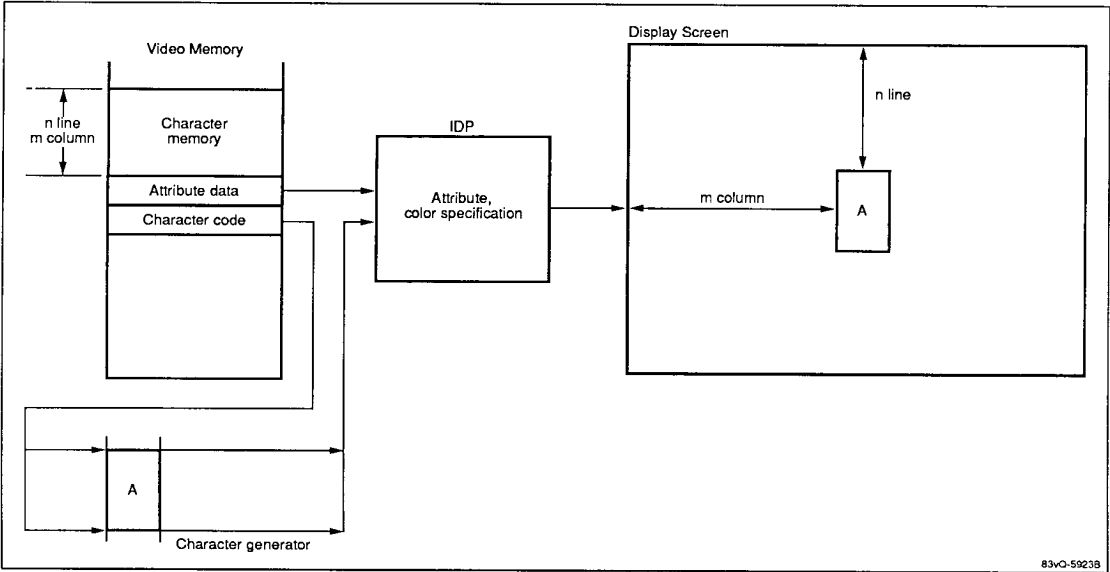
The μPD72022 IDP can control a maximum of 32 sprite images. Collision between sprite images can be detected.

Any desired color pattern (sprite) is displayed at any desired position of the screen based on information in the video memory sprite attribute table. Sprite control commands can change the sprite size, color, display address, display position, etc. See figure 25.

Screen Split Display

The μPD72022 IDP can split the display screen into rectangular windows and display any area extracted from video memory. Each display area is independently controlled by the μPD72022. See figure 26.

Figure 21. Data Flow in Text Mode



3

Figure 22. Data Flow in Semigraphics Mode 0

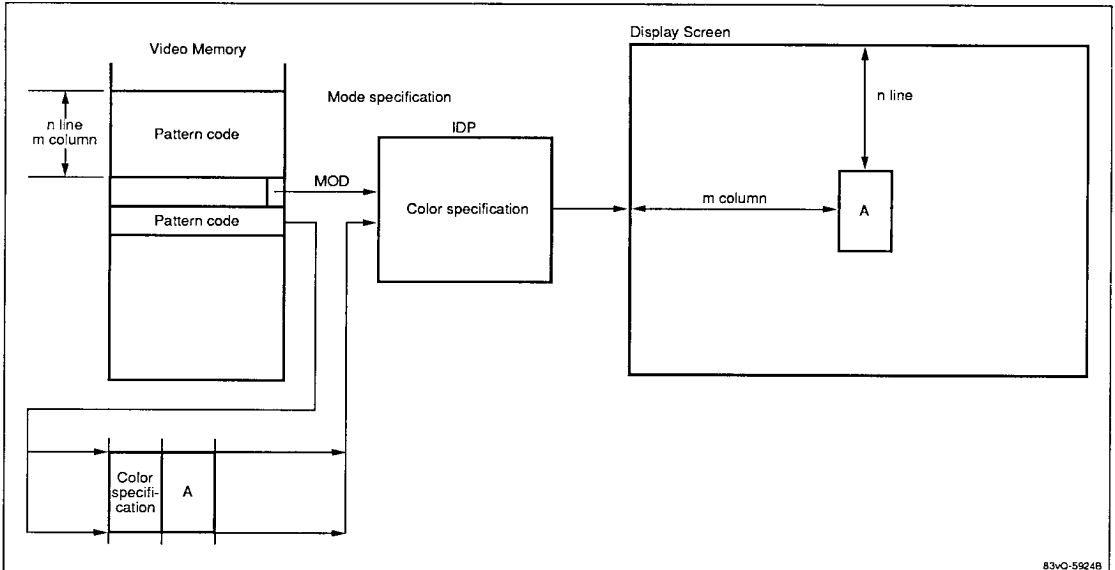


Figure 23. Data Flow in Semigraphics Mode 1

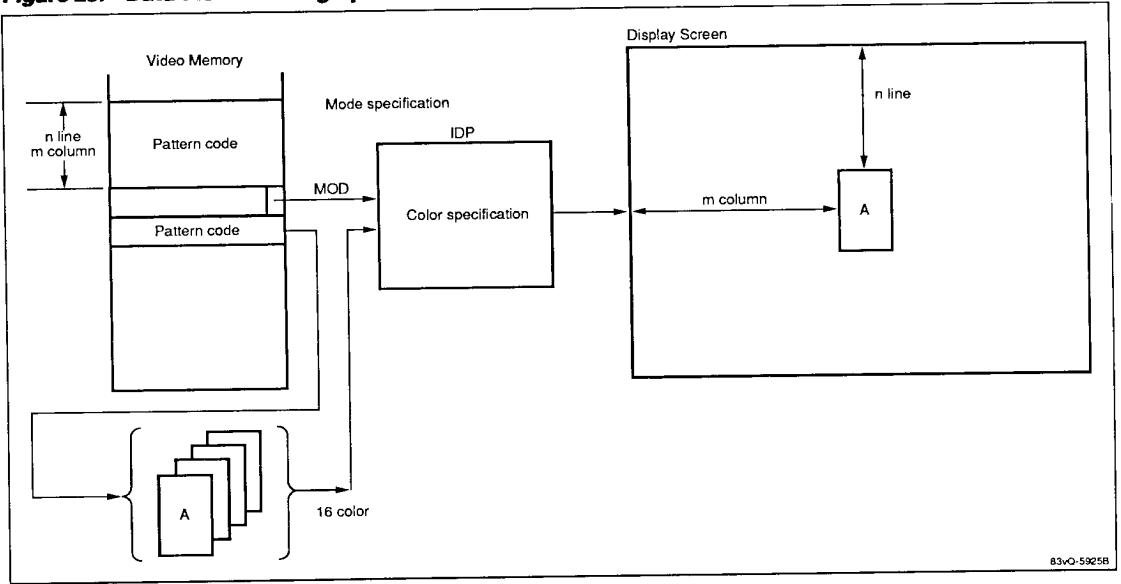


Figure 24. Data Flow in Graphics Mode

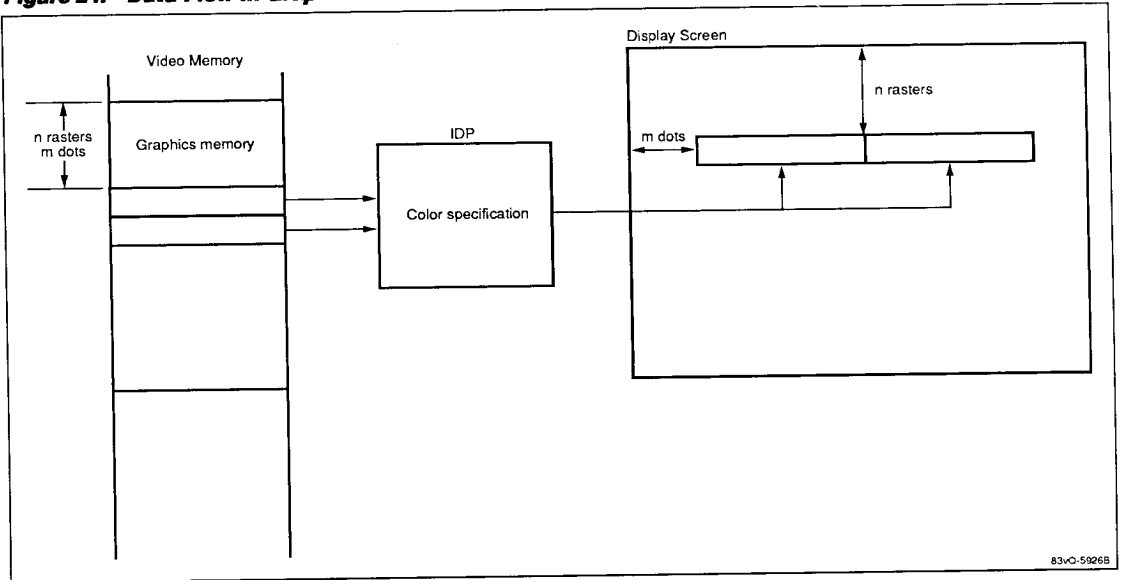


Figure 25. Data Flow During Sprite Image Display

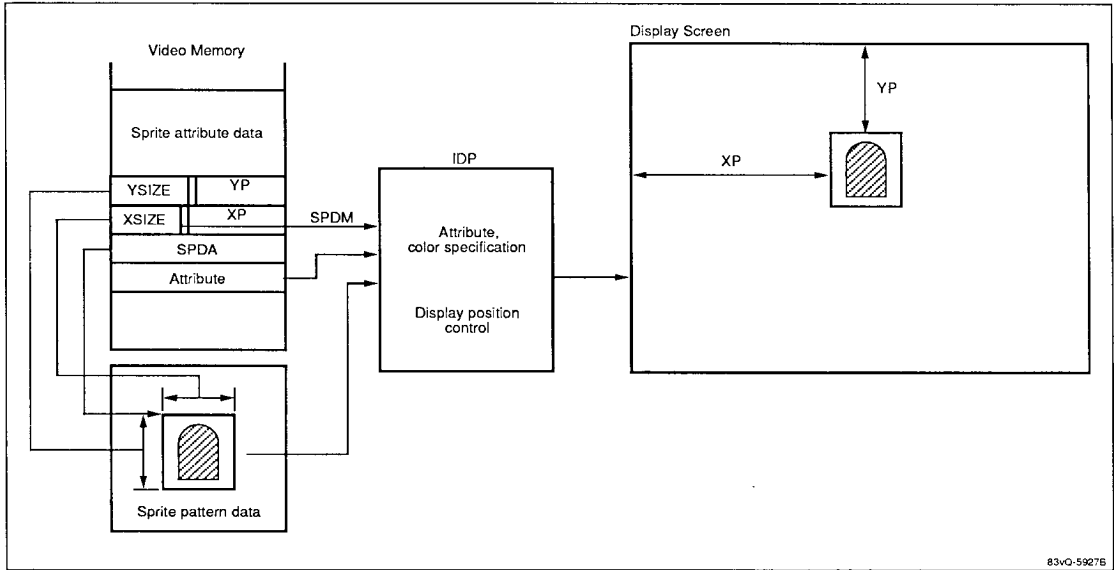
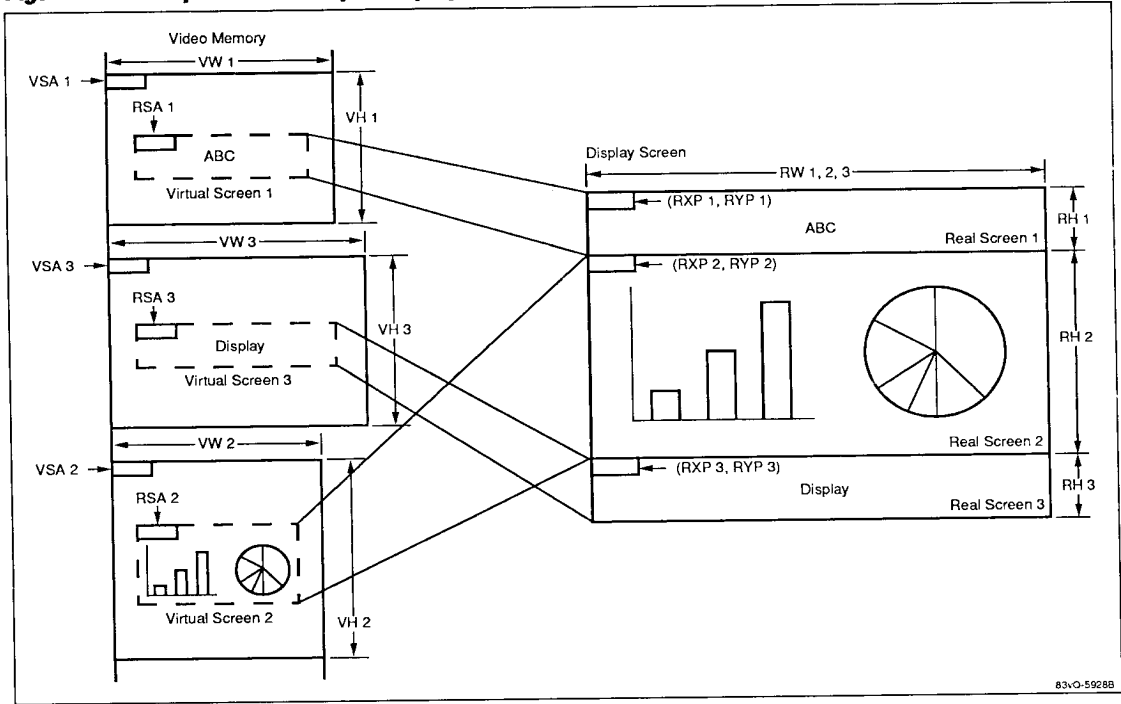


Figure 26. Example of Screen Split Display



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Scan Mode Specification

The μPD72022 IDP enables specification of four scan modes by using SYNC command parameter RM before video signal generation. See figure 27.

Noninterlace Mode. The raster address is incremented for each horizontal scan. The display data address is updated every specified number of rasters.

In graphics mode, the display data address is updated each horizontal scan.

Interlace Mode. Odd and even fields are displayed alternately. In the odd field, the raster address starts at 0; in the even field, it starts at 1. The raster address is incremented by two for each horizontal scan.

In graphics mode, the display address is updated so that display data in the opposite field is skipped.

In interlace mode, the MRA value must be specified so that the number of rasters is even.

To use the interlace mode, a value appropriate for the 16-kHz monitor must be set in the raster parameter and the interlace synchronizing signal must be input from an external source.

Vertical Magnification Mode. The raster address is incremented every two horizontal scans. The display data address is updated every specified number of rasters.

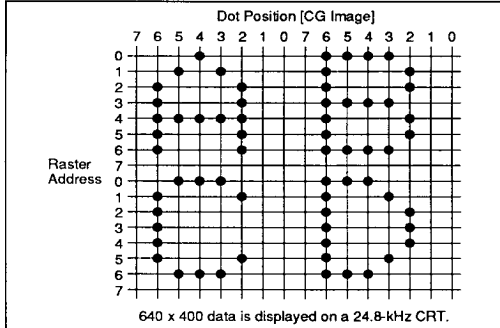
In graphics mode, the display data address is updated every two horizontal scans.

Normal Mode. The raster address is incremented each horizontal scan. The display data address is updated every specified number of rasters.

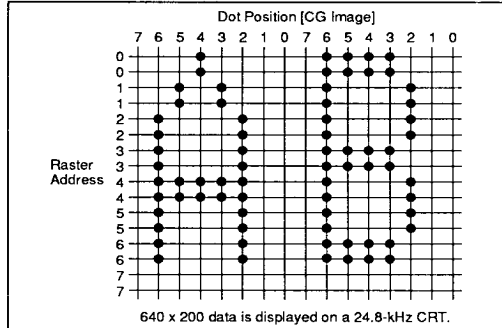
In graphics mode, the display data address is updated each horizontal scan.

Figure 27. Scan Modes

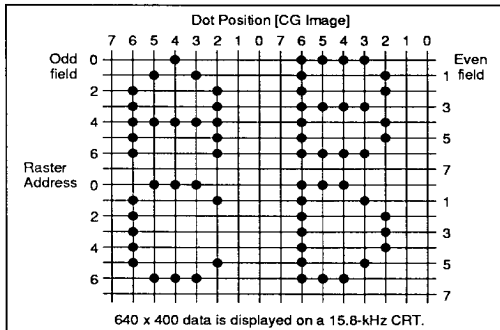
A. Noninterlace Mode



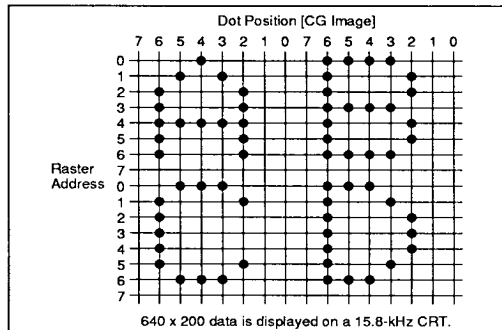
C. Vertical Magnification Mode



B. Interlace Mode



D. Normal Mode



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3